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STE2007

96 x 68 Single Chip LCD Controller/Driver

Features

- 68 x 96 bits Display Data RAM
- 33,49, 65 and 68 Lines Mode
- Row by Row Scrolling
- Interfaces
  - 3-lines Serial Interface (read and write)
  - I^2C (read and write)
  - 4-Line Serial (read and write)
- Partial Display Mode (33,25,17,9 Lines Mode)
- Fully Integrated Oscillator requires no external components
- CMOS Compatible Inputs
- Programmable ID-Number
- Programmable Bias Ratio
- Programmable Columns Organization
- Fully Integrated Configurable LCD bias voltage generator with:
  - Selectable multiplication factor (3x, 4X and 5X)
  - Effective sensing for High Precision Output
  - Eight selectable temperature compensation coefficients
- Designed for chip-on-glass (COG) applications
- Low Power Consumption, suitable for battery operated systems
- Interfaces Supply Voltage range from 1.6 to 3.6V
- High Voltage Generator Supply Voltage range from 2.4 to 3.6V
- Display Supply Voltage range from 3 to 13.2V (T_{amb} = 25°C)

Description

The STE2007 is a low power LCD driver, capable to drive 96 columns and up to 68 lines, designed for monochrome displays.

The STE2007 includes fully integrated bias voltage generator (up to 5x multiplication factor), and internal oscillator, thus reducing to minimum the number of external components required and the current consumption.

The STE2007 features the three standard serial interfaces (3 and 4 lines serial, I^2C interface).

Order codes

Type	Ordering Number
Bumped Dice on Waffle Pack	STE2007DIE2

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1 Introduction

In this document is specified LCD driver for Black&White full graphic displays with a resolution of 96x68, 96x65, 96x49, and 96x33 (ColumnsXRows).

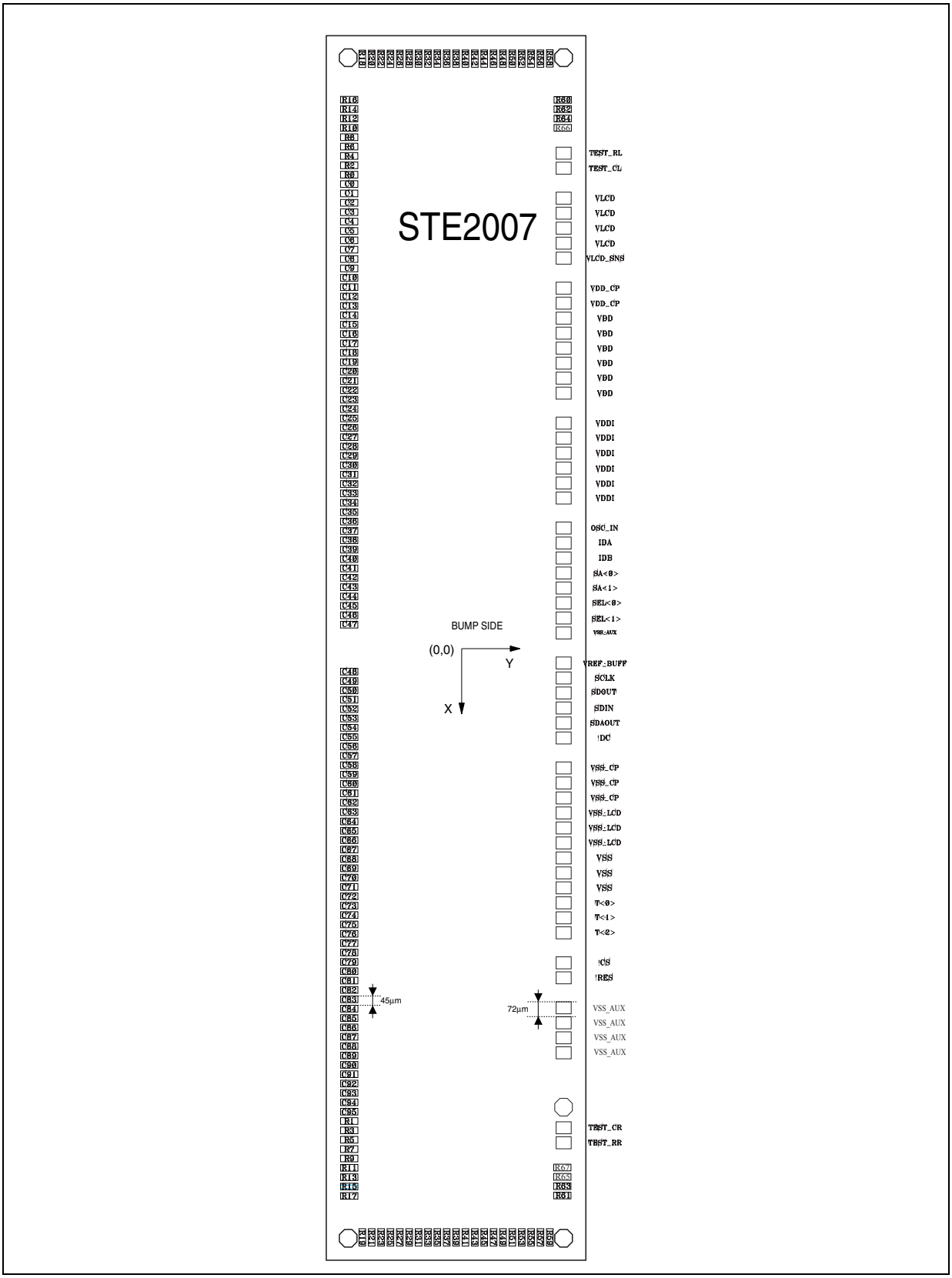
Abbreviations

LCD	Liquid Crystal Display
COG	Chip On Glass –technology
MCU	Micro Controller Unit
DDRAM	Display Data Random Access Memory
MSB	Most Significant Bit
LSB	Least Significant Bit
T.B.D.	To Be Defined

Table 1. General Driver Parameters

Driver assembly technology
Chip On Glass (COG)
Memory Size (Columns x Rows)
96x68 DDRAM capacity: 6528 bits
Mux
1:68 1:65 1:49 1:33
Frame frequency (Hz)
65 70 75 80

Figure 1. Chip Mechanical Drawing



2 Driver Pin Description

2.1 CPU Interface Pins

Table 2. CPU Interface Logic

PIN	Signal	Type	Description	Note
	!RES	I	Reset Input	
	!CS	I	Chip Select Input	When Low the communication port is enabled
	SDOUT	0	Serial Data Output	Must be connected to SDAIN at Module Level
	SDAIN	I	Serial Data Input /I^2C Interface Data Input	
	SCLK	I	Serial Clock Input/I^2C Interface Clock	
	SDA_OUT	0	I^2C Bus Data Out	Must be left floating when I^2C Interface is not is use
	SA1	I	I^2C Slave Address	Cannot be left floating
	SA0	I	I^2C Slave Address	Cannot be left floating
	!D/C	I	4 Line SPI Data/Command Selector	Must be connected to VSSAUX at Module Level when 4-Line SPI is not in USE

2.2 Power Supply Pins

Table 3. Power Supply Pins

PIN	Signal	Type	Description	Note
	VSS	Power	Analog & Digital Grounds	
	VSS_LCD	Power	Drivers Analog Ground	
	VSS_CP	Power	Booster Ground	
	VDDI	Power	Digital Power	
	VDD	Power	Analog Supply	
	VDD_CP	Power	Booster Power Supply	
	VSSAUX	Power	Auxiliar Vss Output	

Table 4. High Voltage Pins

PIN	Signal	Type	Description	Note
	V_{LCD}	High Voltage	Booster Output	Cext = 0.1-1µF Connected to Vss
	V_{LCD_SENSE}	High Voltage	Booster Sense Input	Must be connected to Vlcd at module level

Table 4. High Voltage Pins (continued)

PIN	Signal	Type	Description	Note
	COM0 to COM67	High Voltage	LCD Row Driver Output	Unused lines must be left floating
	COMS	High Voltage	LCD Row Driver Output	Unused lines must be left floating
	SEG0 to SEG95	High Voltage	LCD Column Driver Output	Unused lines must be left floating

2.3 Configuration Pins

Table 5. Configuration Pin Description

<table>
<tr><th>PIN</th><th>Signal</th><th>Type</th><th>Config</th><th>Description</th><th>Note</th></tr>
<tr><td rowspan="2"></td><td rowspan="2">OSCIN</td><td rowspan="2">I</td><td>VSS/VSSAUX</td><td>Internal Oscillator Stopped</td><td rowspan="2"></td></tr>
<tr><td>VDDI</td><td>Internal Oscillator Active</td></tr>
<tr><td></td><td>SEL0 -SEL1</td><td>I</td><td colspan="2"><table><tr><th>SEL1</th><th>SEL0</th><th>Interface</th></tr><tr><td>VSS/VSSAUX</td><td>VSS//VSSAUX</td><td>I^2C</td></tr><tr><td>VSS/VSSAUX</td><td>VDD1</td><td>SPI 4-Lines 8 bit</td></tr><tr><td>VDD1</td><td>VSS/VSSAUX</td><td>Serial 3-Lines 9 bit</td></tr><tr><td>VDD1</td><td>VDD1</td><td>Not Used</td></tr></table></td><td></td></tr>
<tr><td rowspan="2"></td><td rowspan="2">IDA</td><td rowspan="2">I</td><td>VSS/VSSAUX</td><td>IDA=”0”</td><td rowspan="2"></td></tr>
<tr><td>VDDI</td><td>IDA=”1”</td></tr>
<tr><td rowspan="2"></td><td rowspan="2">IDB</td><td rowspan="2">I</td><td>VSS/VSSAUX</td><td>IDB=”0”</td><td rowspan="2"></td></tr>
<tr><td>VDDI</td><td>IDB=”1”</td></tr>
</table>

2.4 Test Pins

Table 6. Test Pin Description

PIN	Signal	Type	Description	Note
	T2	I	Test Input. Enable Test Mode.	Must Be connected to VSS in Normal Working Mode
	T1	I	Test Input. Enable Test Mode.	Must Be connected to VSS in Normal Working Mode
	T0	I	Test Input.	Must Be connected to VSS in Normal Working Mode
	T3	O	Test Output.	Must Be OPEN in Normal Working Mode

Table 6. Test Pin Description (continued)

PIN	Signal	Type	Description	Note
	T4	O	Test Output.	Must Be OPEN in Normal Working Mode
	T5	O	Test Output.	Must Be OPEN in Normal Working Mode
	T6	O	Test Output.	Must Be OPEN in Normal Working Mode
	VREF_BUFF	O	Analog Test Output	Must be left floating

3 Display Driver Electrical Characteristics

3.1 Absolute maximum ratings

Table 7. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDI}	Supply Voltage Range	- 0.5 to + 5	V
V_{DD}	Supply Voltage Range	- 0.5 to + 5	V
V_{LCD}	LCD Supply Voltage Range	- 0.5 to + 14.0	V
I_{SS}	Supply Current	- 50 to +50	mA
V_i	Digital Inputs Voltage	-0.5 to V_{DDI} + 0.5	V
I_{in}	DC Input Current	- 10 to + 10	mA
I_{out}	DC Output Current	- 10 to + 10	mA
P_{tot}	Total Power Dissipation (T_j = 85°C)	300	mW
P_o	Power Dissipation per Output	30	mW
T_j	Operating Junction Temperature	-40 to + 85	°C
T_{stg}	Storage Temperature	- 65 to 150	°C
All pins vs VDDI (*)	ESD Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002- “Human Body Model” Acceptance Criteria: “Normal Performance”	±1750	V
All other pins / pin combination		±2000	V

Note: (*) ESD tests have been performed with VSS, VSS_LCD and VSS_CP shorted together

3.2 DC Characteristics

Table 8. DC characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD},V_{DDCP}	Power Supply Voltage	Operating Voltage	2.4		3.6	V
V_{DDI}	Power Supply Voltage(Logic)	I/O supply Voltage	1.6		3.6	V
V_{LCD}	Booster Output				13.5	V
V_{LCD_SENSE}	Booster Sense Input				13.5	V
V_{LCD}	LCD Supply Voltage Accuracy	V_{LCD}=10V; VDD=2.6V; T_{amb} = 25°C; No display Load; f_{SCLK}=0Hz	-2		2	%
$I(V_{DDI})$	Logic Supply Current	Power Saver Mode ON (Interfaces quiescent)		1	3	µA
		Power Saver Mode OFF (Interfaces quiescent)		6	20	µA
		Write Mode		120	250	µA
$I(V_{DD}+V_{DDCP})$	Analog Supply Current	V_{LCD}=10V;Booster= 5X; f_{SCLK}=0Hz; VDD=2.4V Refresh Rate=75Hz; no display load;T_{amb} = 25°C		90	180	µA
Logic Inputs						
V_{IH}	Logic High level input voltage		$0.7V_{DDI}$		V_{DDI}	V
V_{IL}	Logic Low level input voltage		Vss		$0.3V_{DDI}$	V
I_{IH}	Logic High level input current				1	µA
I_{IL}	Logic Low level input current				-1	µA
Logic Outputs						
V_{OH}	Logic High level output voltage	I_{OUT} = -500µA; VDDI=1.6V	$0.8V_{DDI}$		V_{DDI}	V
V_{OL}	Logic Low level output voltage	I_{OUT} = 500µA; VDDI=1.6V	Vss		$0.2V_{DDI}$	V

Note: 1 T_{amb} = -40 to 85°C, unless otherwise specified.

3.3 AC Characteristics

Table 9. AC Operation - Internal Oscillator

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{FRAME}	Frame Frequency Default	VDDI= 1.6; VDD= 2.9V Rafresh Rate = 75Hz Tamb = -20°C to +70°C	68	75	82	Hz

3.4 MCU Tx Data Mode

Table 10. AC Characteristics for Serial interface

Description	Signal	Symbol	Notes	Min.	Typ.	Max.	Unit
Chip Select	!CS	tcss		60			ns
		tcsh		100			ns
		tchw		50			ns
Input Serial Data Interface	SDAIN	tsds	Data setup time	100			ns
		tsdh	Data hold time	100		125	ns
Output Serial Data interface	SDAOUT	tac	Access Time	0		100	ns
		tod	Output Disable Time	25		100	ns
Serial clock input	SCLK	tscyc	Serial clock cycle	250			ns
		tshw	Serial clock H pulse width	100			ns
		tslw	Serial clock L pulse width	100			ns

Note: 1 The input signal rise and fall times must be within 10ns.

2 Every timing is specified on the basis of 30% and 70% of VDDI.

3 T_{amb} = -40 to 85°C, unless otherwise specified.

Figure 2. MCU TxData timing

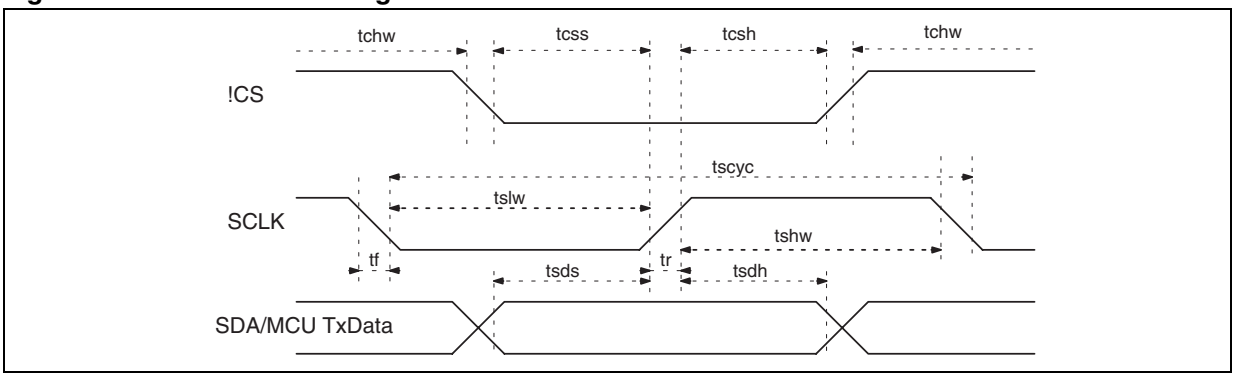


Table 11. Input Signals Change Time

Signal	Symbol	Parameter	Minimum	Typical/ Nominal	Maximum	Unit / Notes
Inputs	tr,tf				10	ns / to 30% & 70% levels

3.4.1 Driver TxData Mode

Table 12. Timings based on 4 MHz SCLK Speed

Item	Symbol	Condition		Rating		Units
			Min.		Max.	
Data hold time	T1	Note 1	100		125	ns
Access time	T2	–	10		100	ns
Output disable time	T3	–	25		100	ns
Data setup time	T4	–	100		–	ns
!CS pulse width high	T5	–	250			ns

Note: 1 Data Hold Time T1 depends on SCLK high time and Max Data Hold time. It is Always 3-8ns before SCLK pulse falling edge

2 The input signal rise and fall times must be within 10ns.

3 Every timing is specified on the basis of 30% and 70% of VDDI.

4 T_{amb} = -40 to 85°C, unless otherwise specified.

Table 13. Timings based on 1 MHz SCLK Speed

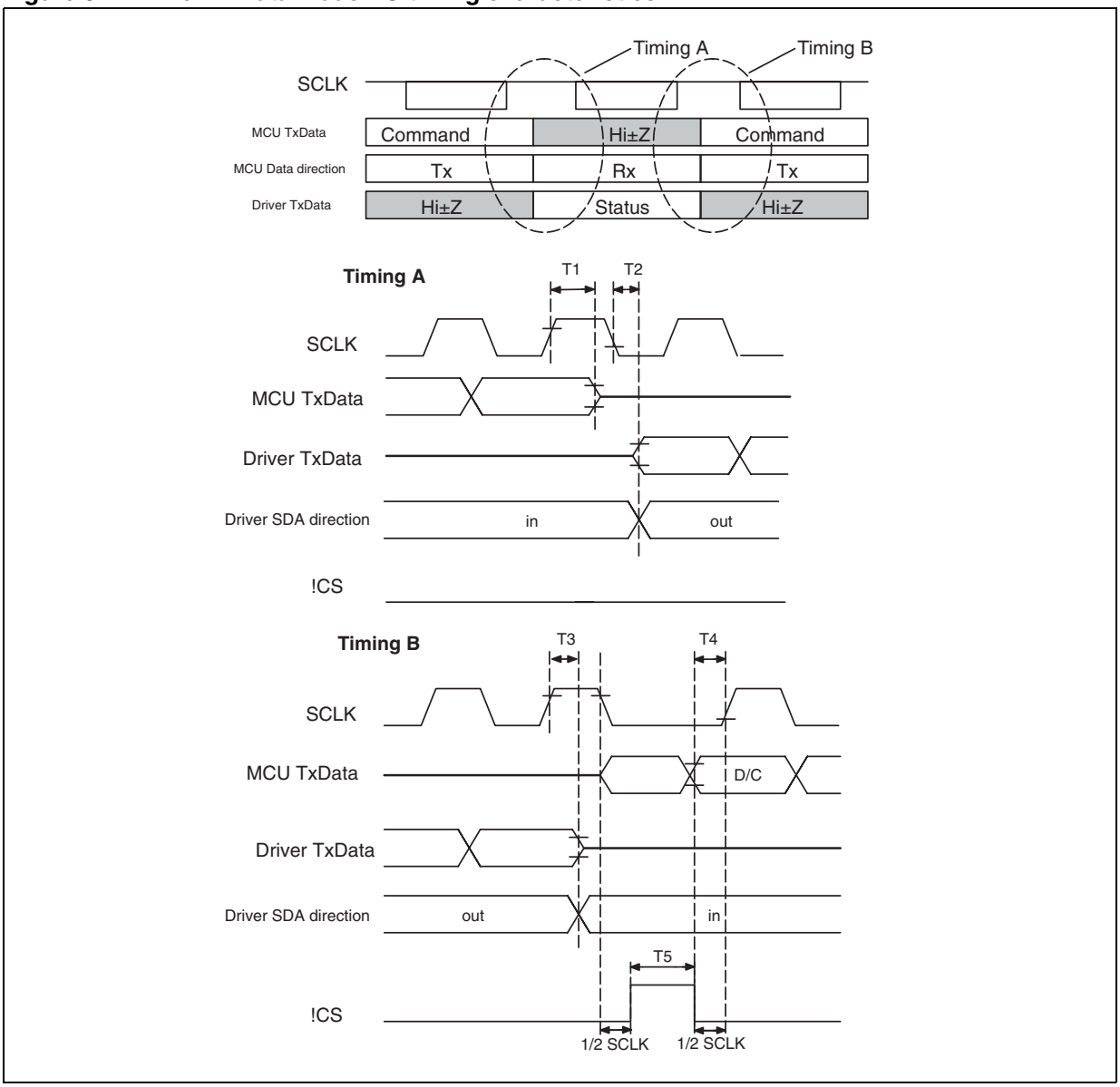
Item	Symbol	Condition		Rating		Units
			Min.		Max.	
Data hold time *)	T1	–	100		125	ns
Access time	T2	–	10		450	ns
Output disable time	T3	–	25		450	ns
Data setup time	T4	–	100		–	ns
1CS pulse width high	T5	–	250			ns

Note: 1 The input signal rise and fall times must be within 10ns.

2 Every timing is specified on the basis of 30% and 70% of VDDI.

3 T_{amb} = -40 to 85°C, unless otherwise specified.

Figure 3. Driver TxData Mode AC timing characteristics



3.4.2 Reset Timing

Table 14. Reset Timing

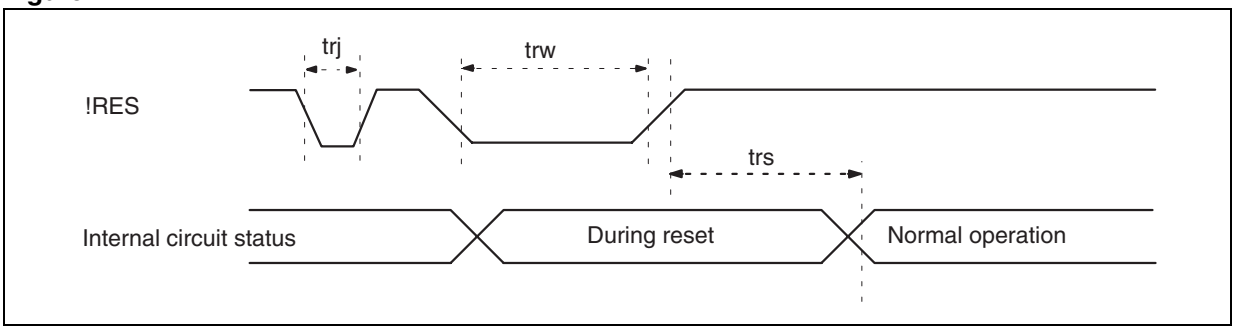
Description	Signal	Symbol	Min.	Max.	Unit
Reset time	!RES	trs		2500	ns
Reset low pulse width (for valid reset)	!RES	trw	2500		
Reset rejection (for noise spike)	!RES	trj		1000	

Note: 1 The input signal rise and fall times must be within 10ns.

2 Every timing is specified on the basis of 30% and 70% of VDDI.

3 T_{amb} = -40 to 85°C, unless otherwise specified.

Figure 4.


trj
trw
!RES
trs
Internal circuit status
During reset
Normal operation

4 INTERFACE

4.1 3-lines 9 bit Serial Interface

STE2007 3-lines 9 bits serial interface is a bidirectional link between the display driver and the host processor.

It consists of three lines:

- SDAIN/SDAOUT Serial Data
- SCLK Serial Clock
- !CS Peripheral enable: - Active Low- Enables and Disables the serial interface

The serial interface is active only if the !CS line is low. If !CS is low after the positive edge of !RES, the serial interface is ready to receive data after the internal reset time. Serial data must be input to SDA in the sequence D/!C, D7 to D0. STE2007 read data on SCLK rising edge. The first bit of serial data D/!C is data/command flag. When D/!C =”1” D7 to D0 bits are display RAM data or Command Parameters. When D/!C=”0” D7 to D0 bits identify a command

4.1.1 MCU TxData Mode (Write Mode)

STE2007 is always a slave device on the communication bus and receive the communication clock on the SCLK pin from the master. Information are exchanged word-wide. Every word is composed by 9 bit. The first bit is named D/!C and indicates whether the following byte is a command (D/!C =0) or a Display Data Byte (D/!C =1).

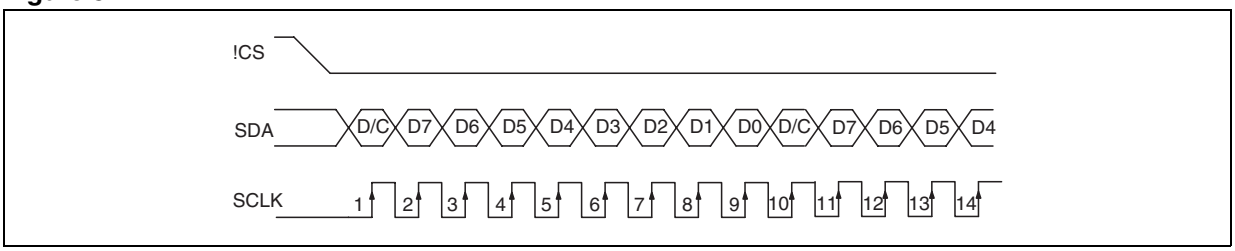
During data transfer, the data line is sampled by the receiver unit on the SCLK rising edge.

The data/command received is transferred to DDRAM or Executed on the first falling edge after the latching rising edge or on the !CS rising edge.

If !CS stays low after the last bit of a command/data byte, the serial interface expects the D/!C bit of the next data byte on the next SCLK positive edge.

A reset pulse on !RES pin interrupts any transmission.

Figure 5.

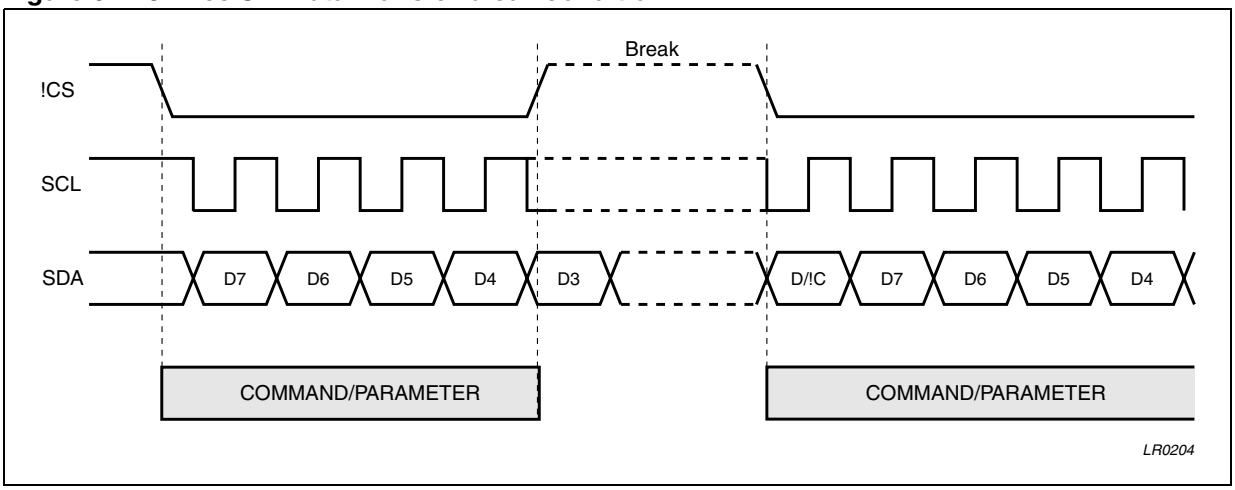


4.1.1.1 Data/Command Transfer break

If the Host processor generates an break condition (!CS Line HIGH before having received Bit D0) while transferring a Data byte to the Frame Memory or a Command identifier or a command parameter, the not complete received byte is discarded, the communication is interrupted and the interface is forced in reset state.

When !CS line becomes low again to start a new communication session STE2007 is ready to receive the same byte interrupted re-transmitted or a new command identifier.

Figure 6. 3-lines SPI Data Transfer break condition



4.1.1.2 Data/Command Transfer pause

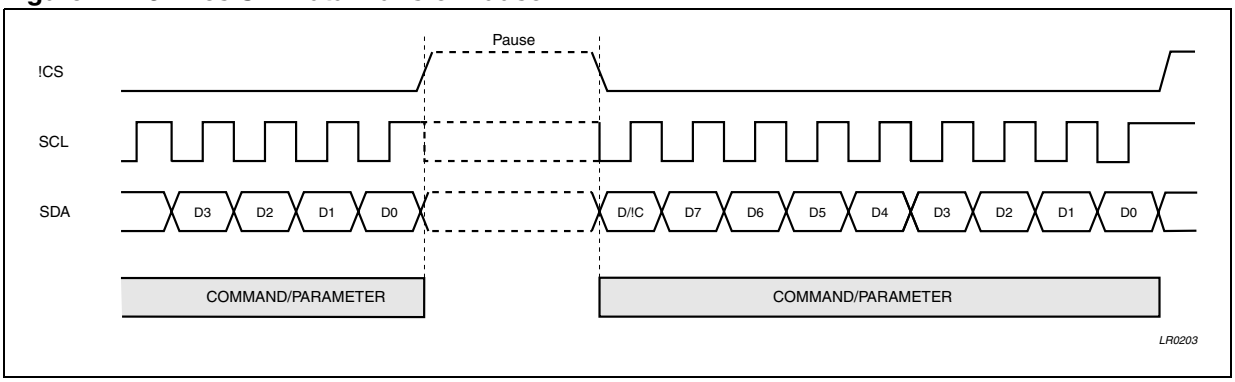
It is possible while transferring Frame Memory Data, Commands or Command Parameters to insert a pause in the data transmission (!CS Line HIGH after 8 Bits Received). When !CS is forced high after a whole byte received, the received byte is processed. Then STE2007 is forced in a wait state ready to restart processing incoming data from the point where the communication has been paused

If a new command identifier is transferred after a pause condition the previous communication session is definitively closed.

Four are the possible conditions:

- Command-Pause-Command
- Command-Pause-Parameter
- Parameter-Pause-Command
- Parameter-Pause-Parameter

Figure 7. 3-lines SPI Data Transfer Pause



4.1.2 Driver TxData Mode (Read Mode)

The Driver TxData–mode is a method to check the electrical interconnection between LCD driver and baseband, to identify the driver and for VDD Intercfonnection electrical self testing.

Self Testing of the electrical contacts is based on the monitoring of VLCD. The improper electrical contact on VDD can be noted from a too low level of VLCD.

The serial interface Driver TxData–mode is controlled by three input signals.

The serial data output (SDAOUT/Driver TxData) and serial clock input (SCLK) are enabled when !CS is low after having received one Reading Command.

To access Driver TxData–mode a Reading command must be sent to STE2007 driver. The first bit (D/C) is low to indicates next 8–bits are for command. The data is read to the driver on the rising edge of SCLK (see section ”MCU TxData–mode”). After last command bit (bit 0) is read SDAOUT becomes active (Low impedance) and MCU is able to read data from driver.

SDAOUT is forced in high impedence when !CS line is forced high or after the eight SCLK rising edges from the last SCLK rising edge of teh reading command transfer (Figure 8).

After sending out all 8 bits the driver release automatically the bus and go back to the MCU TxData–mode. MCU Txdata line changes from high–z to active low or high in the falling edge of 8th SCLK pulse. !CS must be set high and low again before !D/C writing can continue.

If !CS is forced high during the Driver TxDAta-mode, the Driver Tx data session is aborted and SDAOUT is forced in high impedance Mode.

SDAOUT and SDAIN line can be short circuited in normal working conditions.

Figure 8. AC timing characteristics

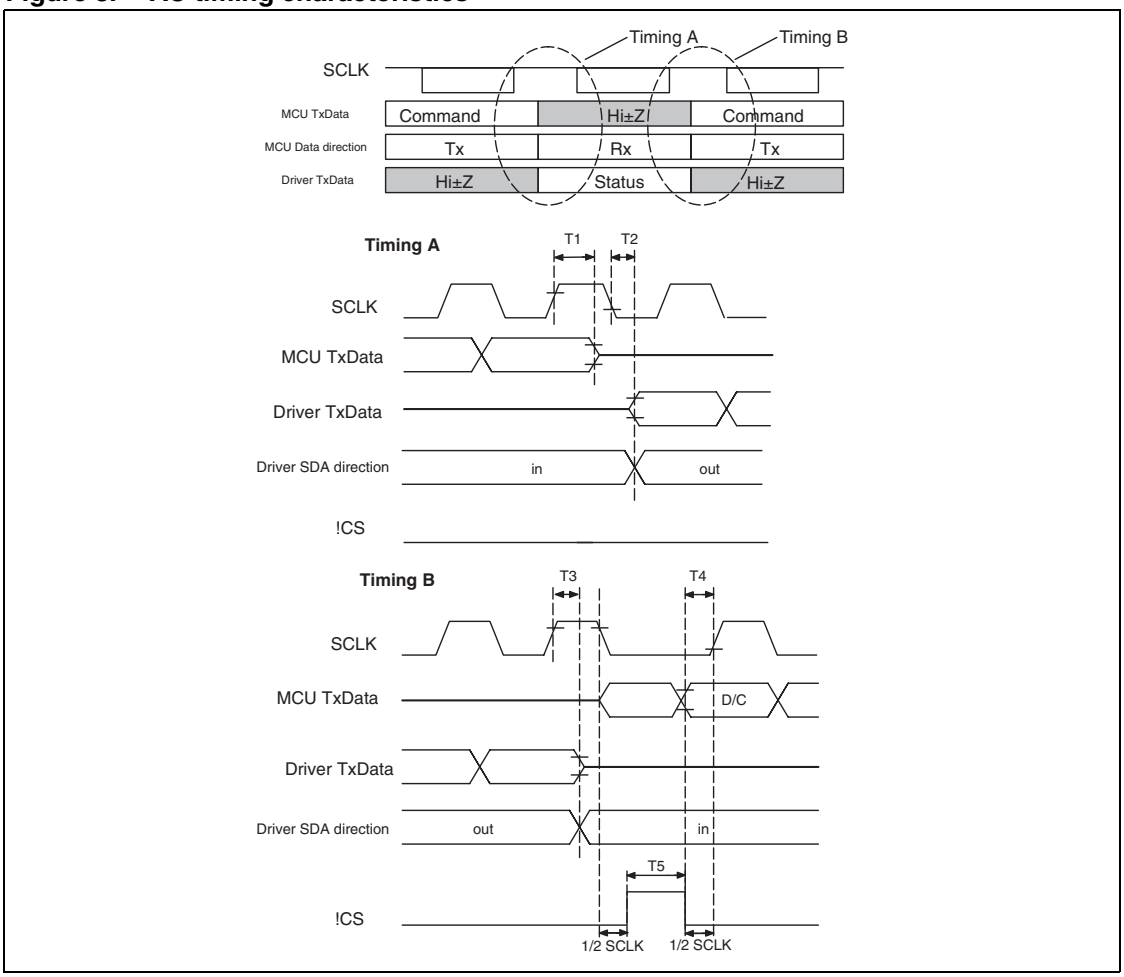
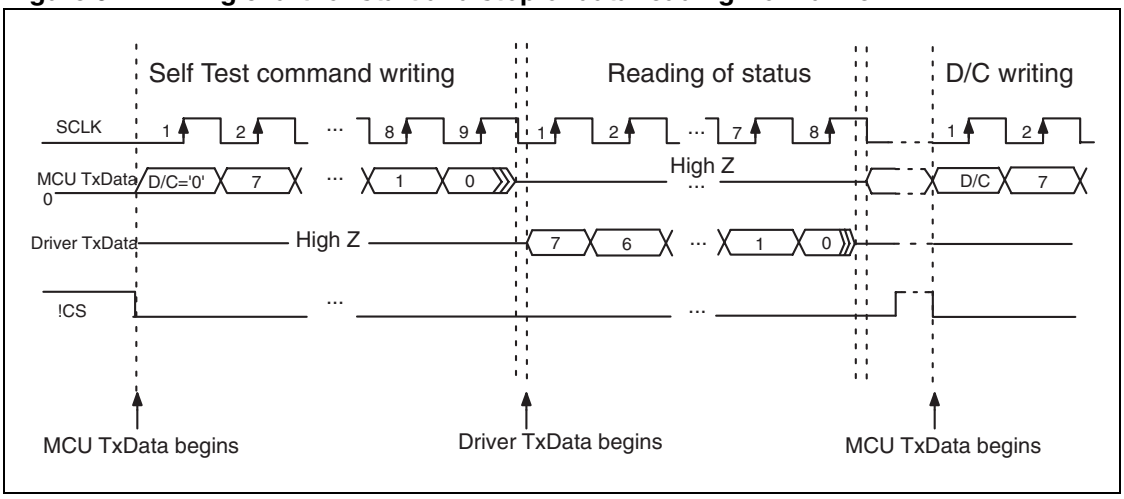


Figure 9. Timing chart for start and stop of data reading from driver



4.2 4-Line SPI

STE2007 4-lines serial interface is a bidirectional link between the display driver and the host processor.

It consists of four lines:

- SDA Serial Data
- SCL Serial Clock
- !CS Peripheral enable: - Active Low- Enables and Disables the serial interface
- Mode selection (D/!C).

The serial interface is active only if the !CS line is low. If !CS is low after the positive edge of !RES, the serial interface is ready to receive data after the internal reset time.

4.2.1 MCU TxData Mode (Write Mode)

STE2007 is always a slave device on the communication bus and receive the communication clock on the SCL pin from the master. Information are exchanged byte-wide. During data transfer, the data line is sampled by the receiver unit on the SCL rising edge.

D/!C line status set whether the byte is a command (D/!C =0) or a data (D/!C =1); D/!C line is read on the eighth SCL clock pulse during every byte transfer.

If !CS stays low after the last bit of a command/data byte, the serial interface expects the MSB of the next data byte on the next SCL positive edge.

If !CS line is forced high in the middle of a data transfer, not complete Data bytes and Commands bytes are discarded.

A reset pulse on !RES pin interrupts any transmission.

Figure 10. 4-lines SPI Commands Transfe

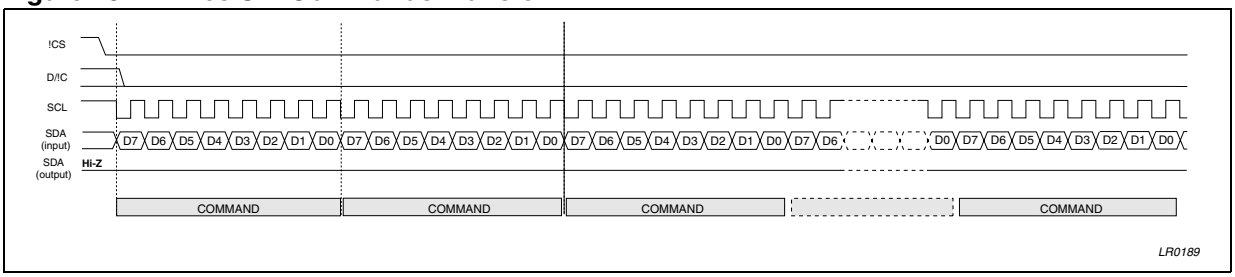
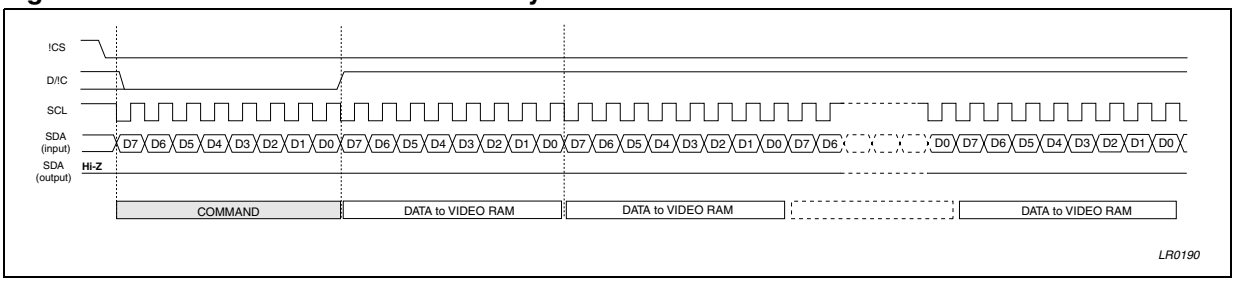


Figure 11. 4-lines SPI Video Data Write Cycle

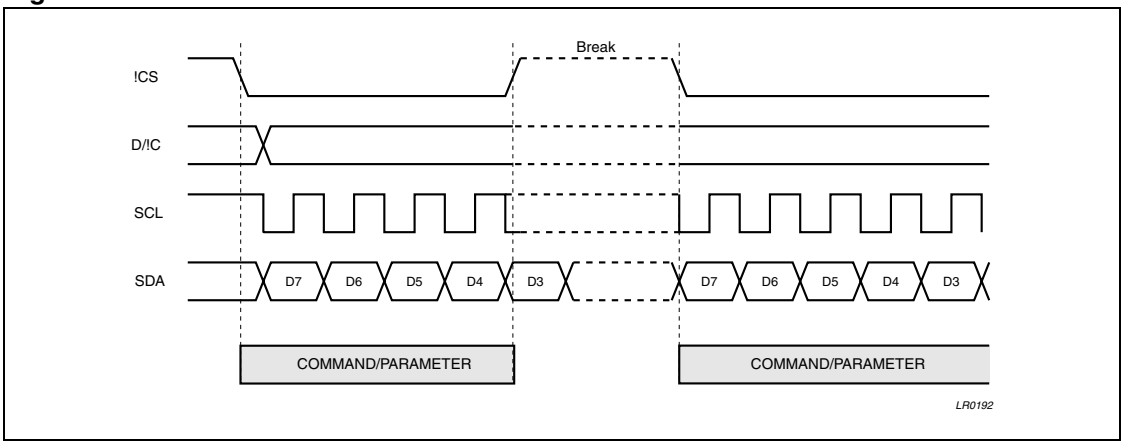


4.2.1.1 Data/Command Transfer break

If the Host processor generates an break condition (!CS Line HIGH before having received Bit D0) while transferring a Data byte to the Frame Memory or a Command identifier or a command parameter, the not complete received byte is discarded, the communication is interrupted and the interface is forced in reset state.

When !CS line becomes low again to start a new communication session STE2007 is ready to receive the same byte interrupted re-transmitted or a new command identifier.

Figure 12. 4-lines SPI Data Transfer break condition



4.2.1.2 Data/Command Transfer pause

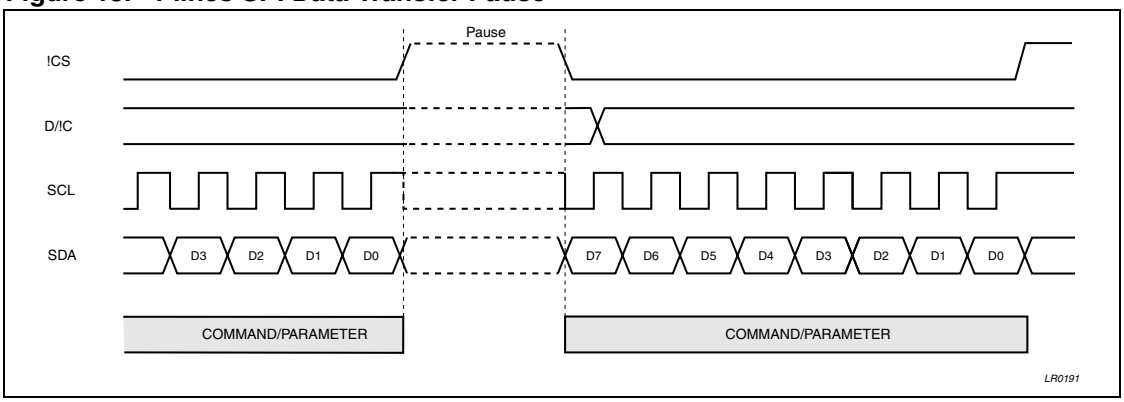
It is possible while transferring Frame Memory Data, Commands or Command Parameters to insert a pause in the data transmission (!CS Line HIGH after 8 Bits Received). When !CS is forced high after a whole byte received, the received byte is processed. Then STE2007 is forced in a wait state ready to restart processing incoming data from the point where the communication has been paused

If a new command identifier is transferred after a pause condition the previous communication session is definitively closed.

Four are the possible conditions:

– Command-Pause-Command
– Command-Pause-Parameter
– Parameter-Pause-Command
– Parameter-Pause-Parameter

Figure 13. 4-lines SPI Data Transfer Pause

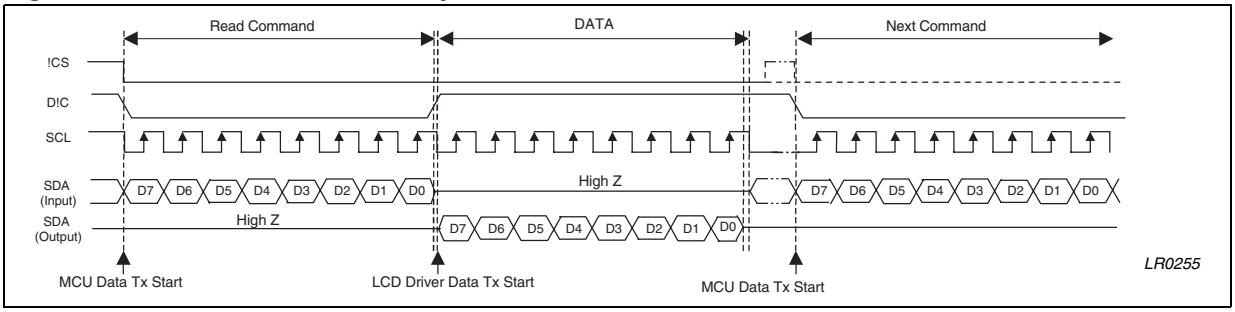


4.2.2 Driver TxData Mode (Read Mode)

Throughout SDA line is possible to read some registers value (ID Numbers, Status byte, temperature).

SDA (output Driver) is in High impedance in steady state and during data write.

Figure 14. 4-lines SPI 8Bit Read Cycle



4.3 I²C Bus

The I²C interface is a fully complying I2C bus specification, selectable to work in both Fast (400kHz Clock) and High Speed Mode (3.4MHz).

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop Data Transfer condition (see below).

Accordingly, the following bus conditions have been defined:

BUS not busy: Both data and clock lines remain High.

Start Data Transfer: A change in the state of the data line, from High to Low, while the clock is High, define the START condition.

Stop Data Transfer: A Change in the state of the data line, from low to High, while the clock signal is High, defines the STOP condition.

Data Valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer starts with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and the stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with the ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the signals is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves"

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA_IN line during the acknowledge clock pulse. Of course, setup and hold time must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Connecting SDA_IN and SDA_OUT together the SDA line become the standard data line. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the STE2007 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

To be compliant with the I^2C-bus Hs-mode specification the STE2007 is able to detect the special sequence "S00001xxx". After this sequence no acknowledge pulse is generated.

Since no internal modification are applied to work in Hs-mode, the device is able to work in Hs-mode without detecting the master code.

Figure 15. Bit transfer and START,STOP conditions definition

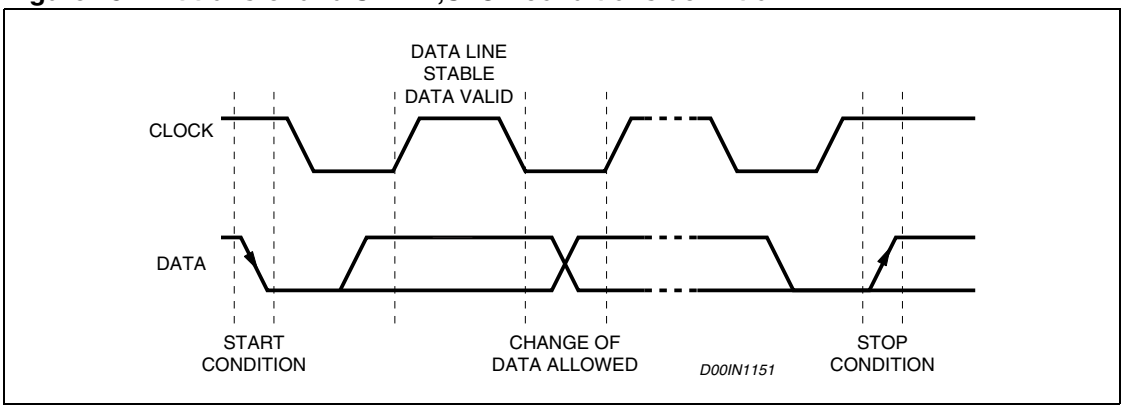
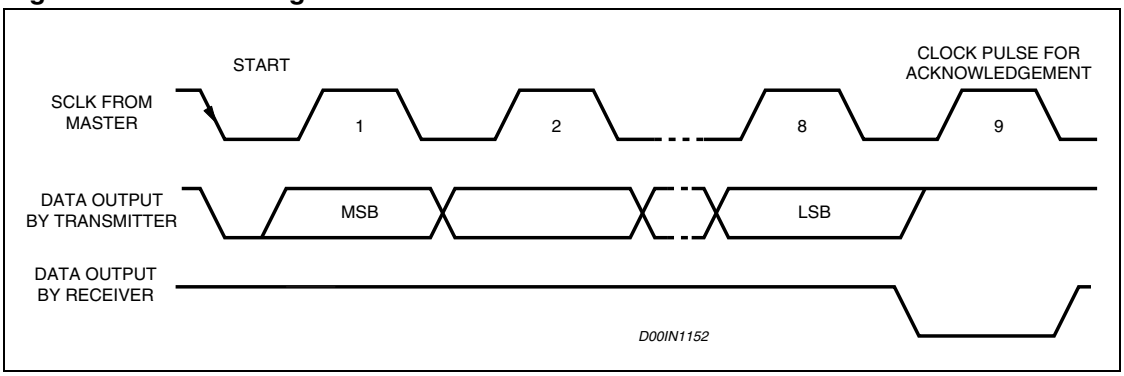


Figure 16. Acknowledgment on the I²C-bus



4.3.1 Communication Protocol

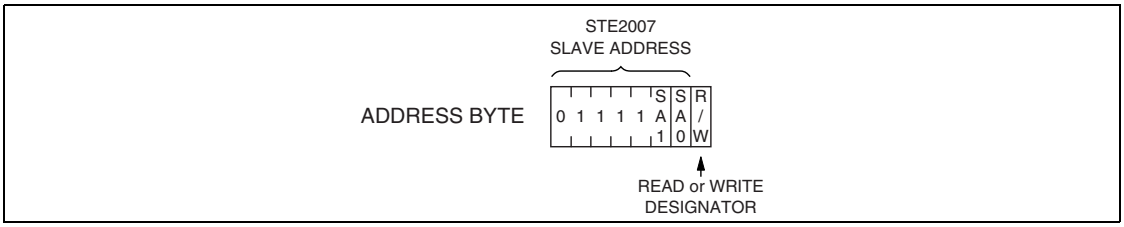
The STE2007 is an I²C slave. The access to the device is bi-directional since data write and status read are allowed.

Four are the device addresses available for the device. All have in common the first 5 bits (01111). The two least significant bit of the slave address are set by connecting the SA0 and SA1 inputs to a logic 0 or to a logic 1.

4.3.2 Starting the Communication

To start the communication between the bus master and the slave LCD driver, the master must initiate a START condition. Following this, the master sends an 8-bit byte, on the SDA bus line (Most significant bit first). This consists of the 7-bit Device Address Code, and the 1-bit Read/ Write Designator (R/$\overline{W}$). The R/$\overline{W}$ bit has to be set to logic 1 to logic 0 according to the type of communication (read or write).

All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.



4.3.3 MCU TxData Mode (Write Mode)

If the R/W bit is set to logic 0 the STE2007 is set to be a receiver and the master can send commands or data.

After the communication has started and slaves have acknowledged, the master sends a control byte defined as follows and waits for its acknowledgement:

CONTROL BYTE	Co	DC	0	0	0	0	0	0

The Co bit is the control byte MSB and defines if after this control byte will follow a single byte sequence (Co = 1) or a multiple bytes sequence (Co = 0). The D/$\overline{C}$ bit defines whether the following byte (if Co = 1) or the following stream of bytes (if Co = 0) are command (D/$\overline{C}$ = 0) or DDRAM data (D/$\overline{C}$ = 1).

Depending on state of flags Co and D/C, four writing sequences are possible:

SINGLE COMMAND BYTE SEQUENCE (Co = 1, D/$\overline{C}$ = 0): a single byte interpreted as a command will follow the control byte;

SINGLE DATA BYTE SEQUENCE (Co = 1, D/$\overline{C}$ = 1): a single byte interpreted as a data to be written in DDRAM will follow the control byte;

MULTIPLE COMMAND BYTES SEQUENCE (Co = 0, D/$\overline{C}$ = 0): a stream of bytes will follow the control byte, with each single byte interpreted as a command;

MULTIPLE DATA BYTES SEQUENCE (Co = 0, D/$\overline{C}$ = 1): a stream of bytes will follow the control byte, with each byte interpreted as a data byte to be written in DDRAM.

Every single byte of a sequence must be acknowledged by all addressed units.

A multiple data sequence is terminated only by sending a STOP condition on the I^2C bus.

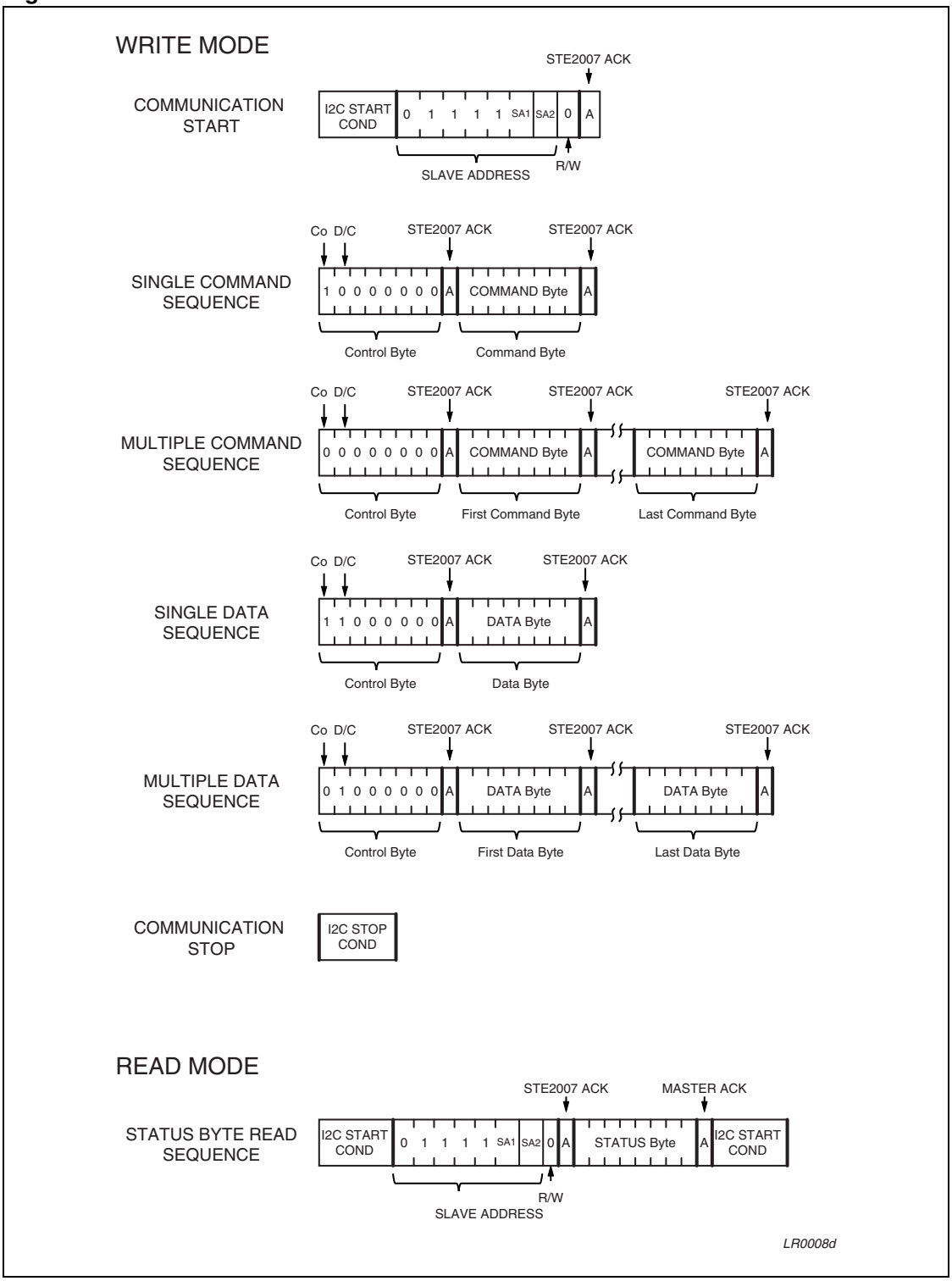
When a sequence is terminated, another sequence of any type can follow or a I^2C STOP condition can be sent to close the communication.

In a single or multiple data bytes sequence, every data byte received is stored in the DDRAM at the location specified by the current values of data pointers. Data pointers are automatically updated after each single data byte written.

4.3.4 Driver TxData Mode (Read Mode)

If the R/W bit is set to logic 1 the chip will output data immediately after the slave address. If the D/C bit during the last write access, is set to a logic 0, the byte read is the status byte.

Figure 17. Communication Protocol



4.4 Reading Mode

STE2007 features a reading Command to transmitt data from the LCD driver to Host Processor. After the reading command STE2007 transfers 8 bits to the Host controller:

– Identification Byte (Command Code DB_{hex})

4.4.1 IIdentification byte

Identification byte is an 8 Bit code that identify the module revision Number.

Table 15. ID byte format

Bit nr	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
	0	0	IDB PAD	IDA PAD	0	0	0	0

Figure 18.

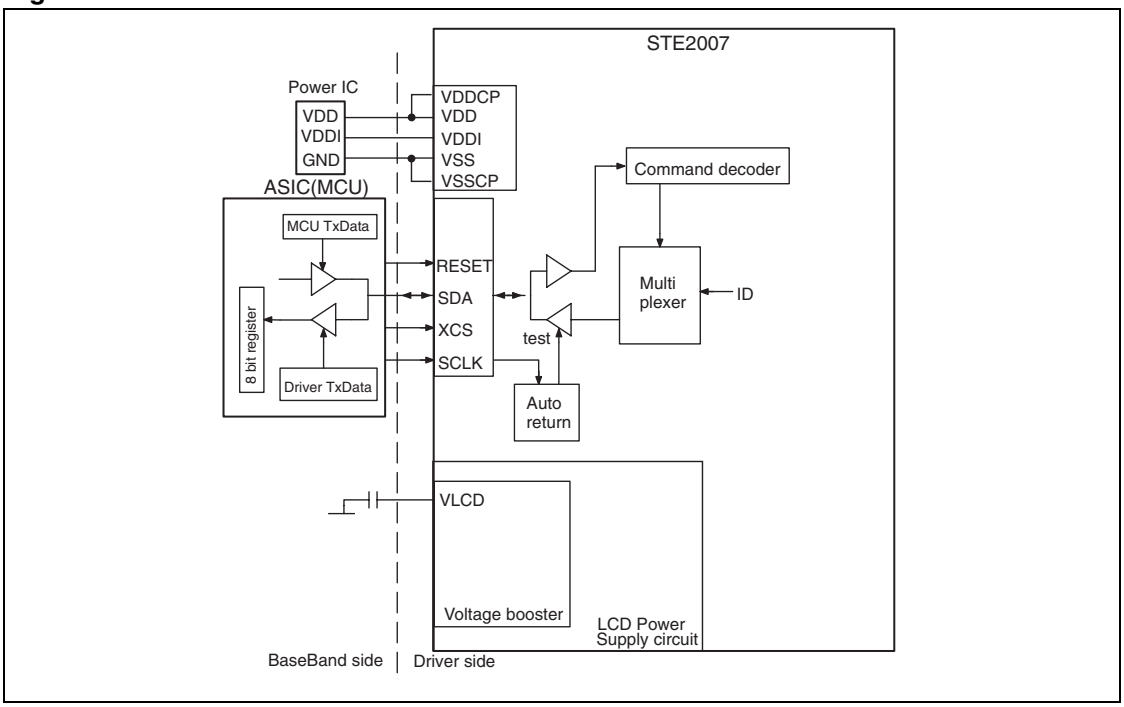
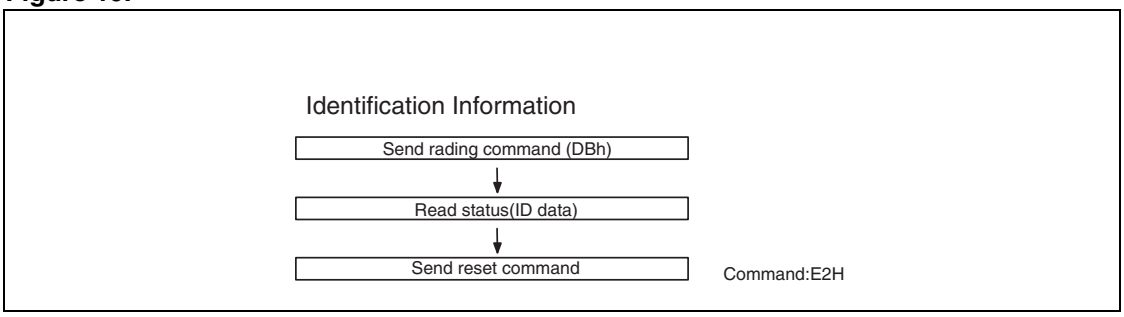


Figure 19.

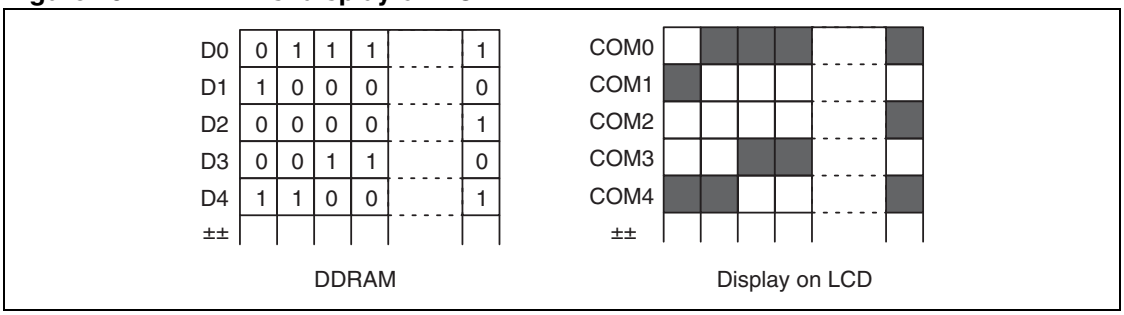


5 Display Data RAM (DDRAM)

5.1 DDRAM and Page/column address circuit

The DDRAM stores pixel data for LCD. It is a 68–row (8 page by 8 bits +4) by 96–column addressable array. D7 to D0 display data from MCU corresponds to the LCD common direction. ”0” bit in DDRAM is a OFF–dot on display and ”1” bit in DDRAM is displayed as ON–dot on display.

Figure 20. DDRAM vs. display on LCD



Each pixel can be selected when page address and column address are specified. The MCU issues Page address set command to change the page and access to another page. In DDRAM page address 8 (D3,D2,D1,D0=1,0,0,0) only display data D0,D1,D2 & D3 are valid.

The DDRAM column address is specified by Column address set command.

The specified column address is automatically incremented by +1 when a Display data write command is entered. After the last column address (5Fh), column address returns to 00h and page address incremented by +1. After the very last address (column=5Fh, page=8h), both column address and page address return to 00h (column address=00h, page address=0h).

Figure 21. Column address in normal mode

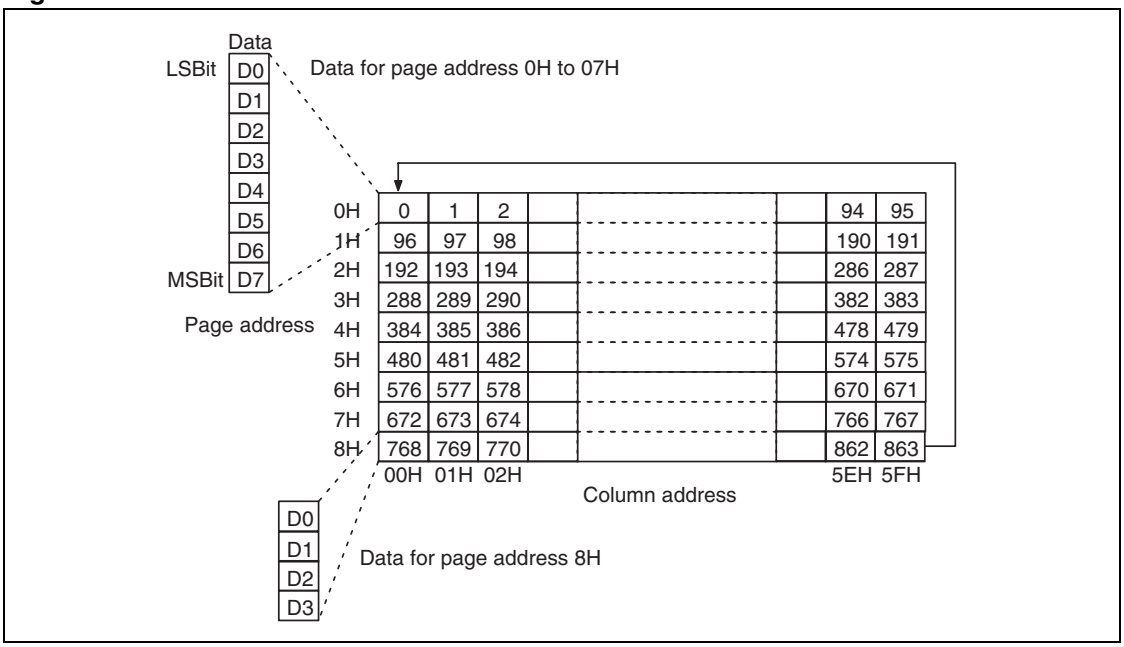
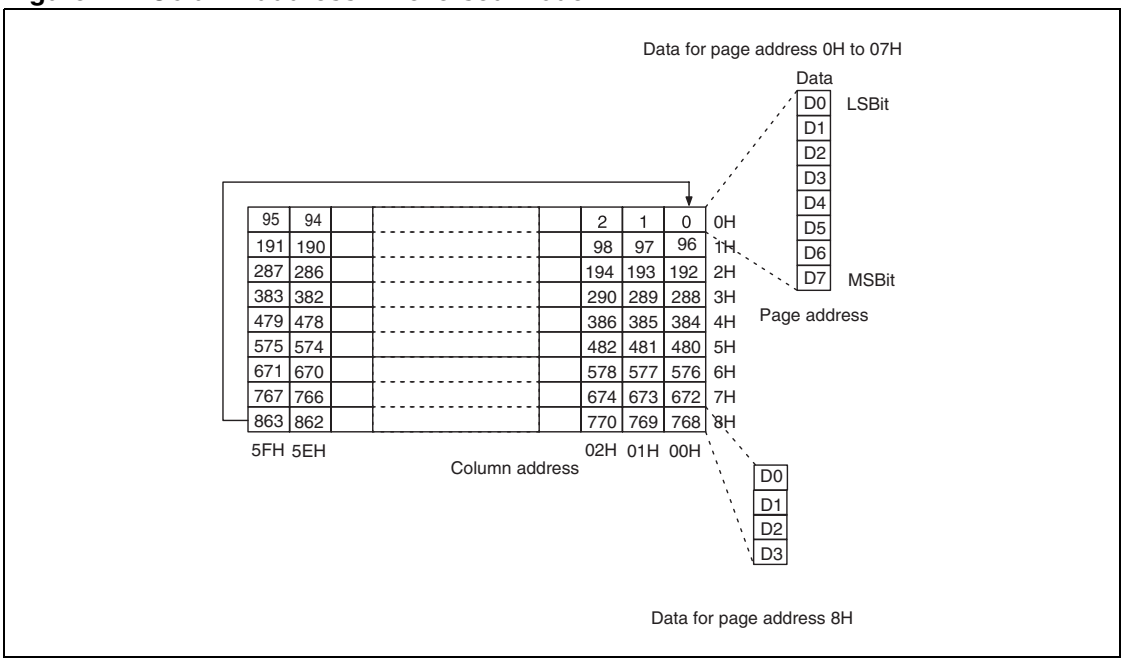


Figure 22. Column address in reversed mode



Data can be written to the DDRAM at the same time as data is being displayed, without causing the LCD to flicker.

Segment driver direction command can be used to reverse the relationship between the DDRAM column address and segment output. This function is achieved writing data into DDRAM in reverse order (from Right to left).

Table 16. Column address direction

Column address	00H	01H	02H	5DH	5EH	5FH	5DH
Normal Direction	SEG0	SEG1	SEG2	_ _ _ _ _ _	SEG93	SEG94	SEG95
Reverse Direction	SEG95	SEG94	SEG93	_ _ _ _ _ _	SEG2	SEG1	SEG0

5.2 Line address circuit

The line address circuit specifies the line address relating to the COM output when the contents of the DDRAM are displayed. The display start line that is normally the top line of the display, can be specified by Display start line address set command.

STE2007 features Four different Multiplexing Mode to fine tune the duty ratio on the display size:

- 68 Lines Display
- 65 Lines Display
- 49 Lines Display
- 33 Lines Display

Figure 23. 68–line Mode

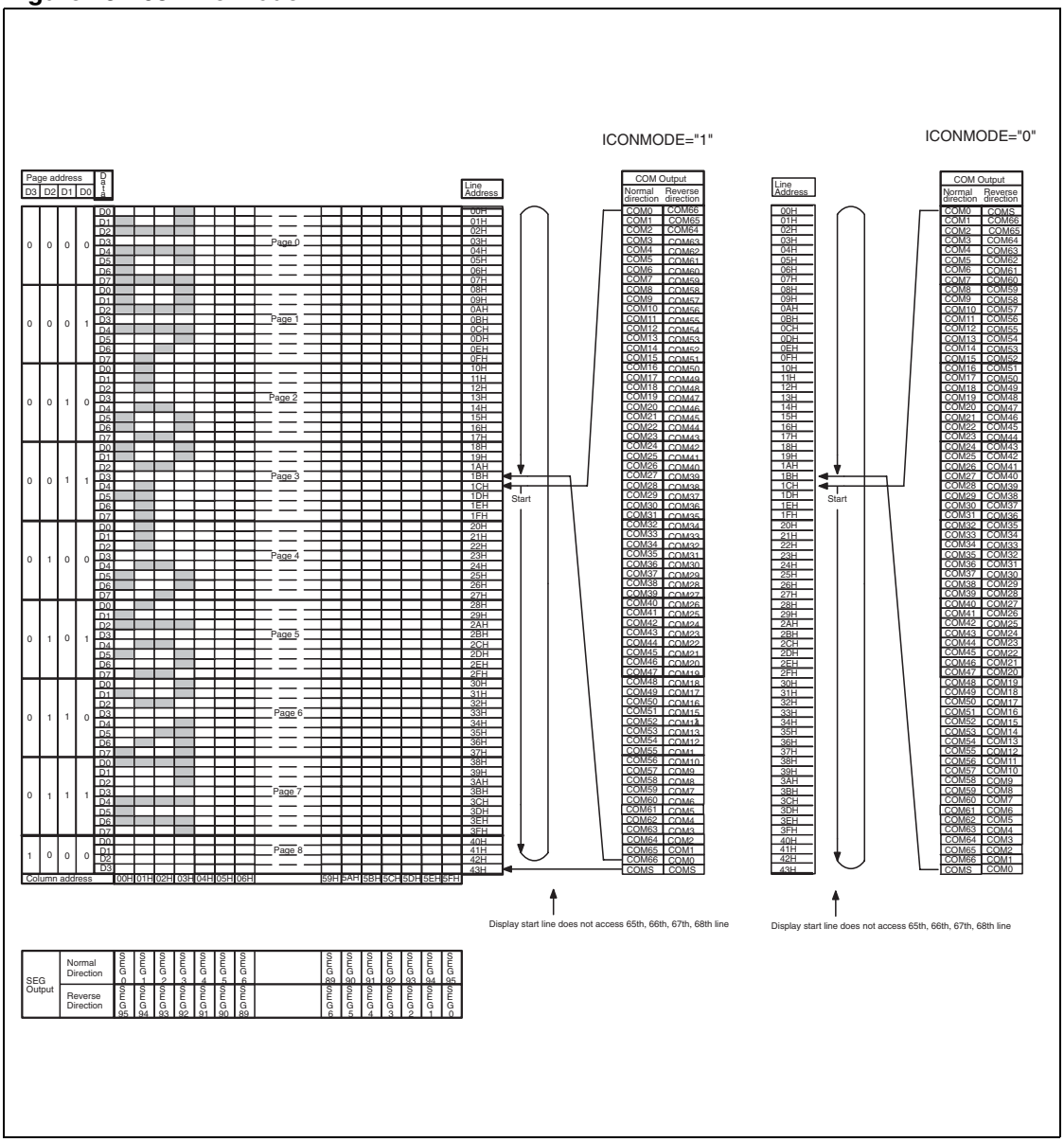


Figure 24. 65–line Mode

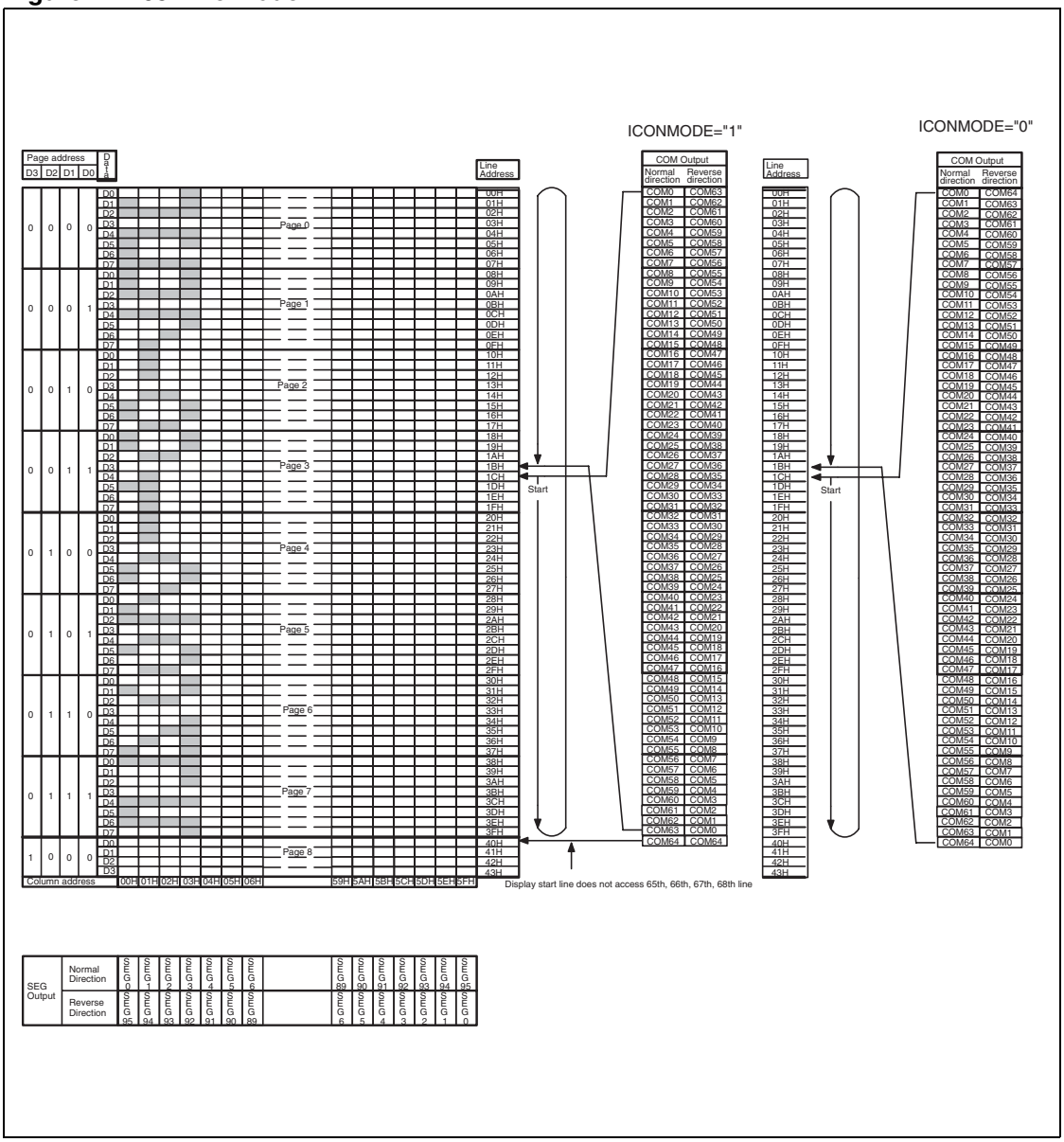


Figure 25. 49–line Mode

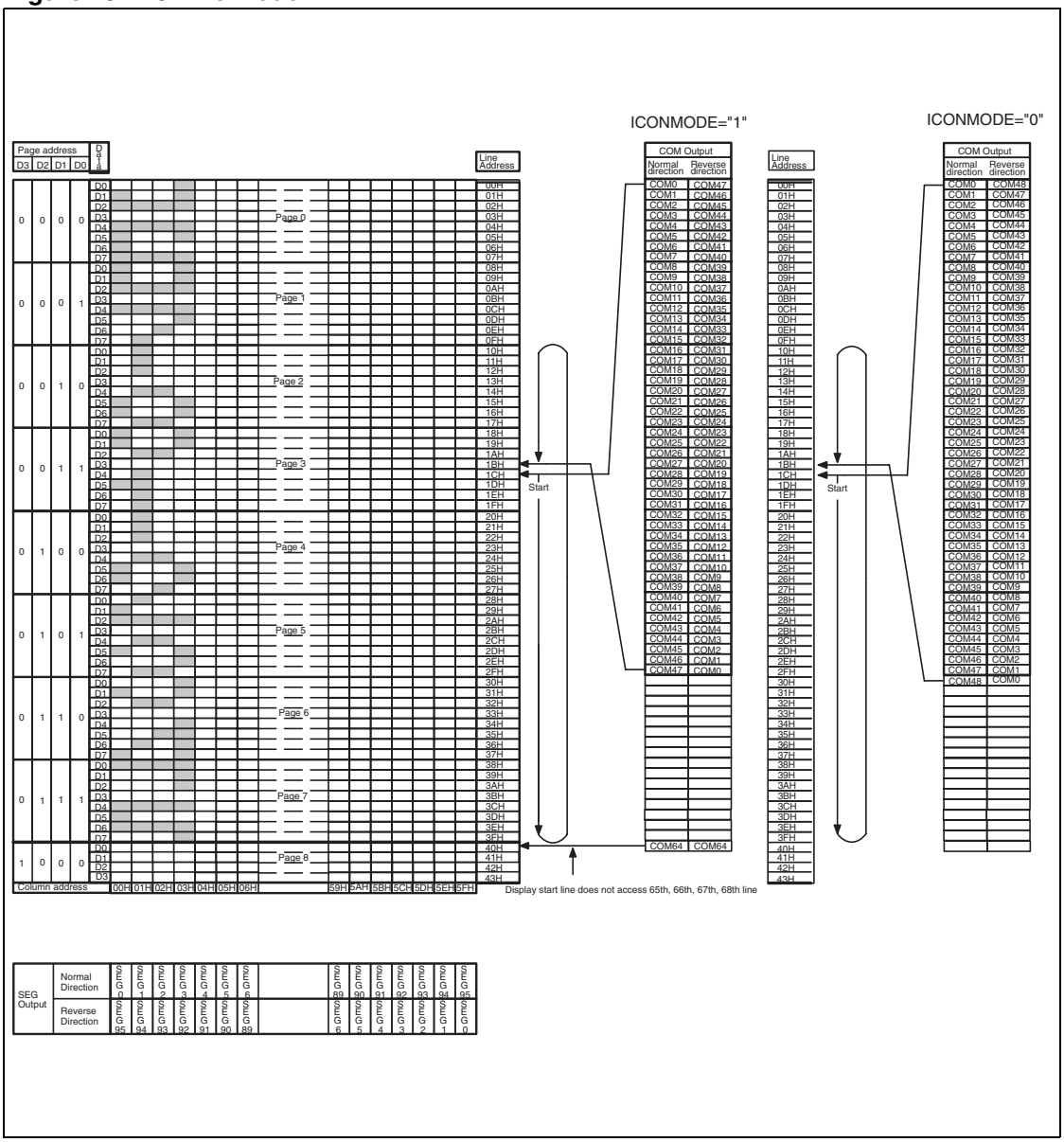
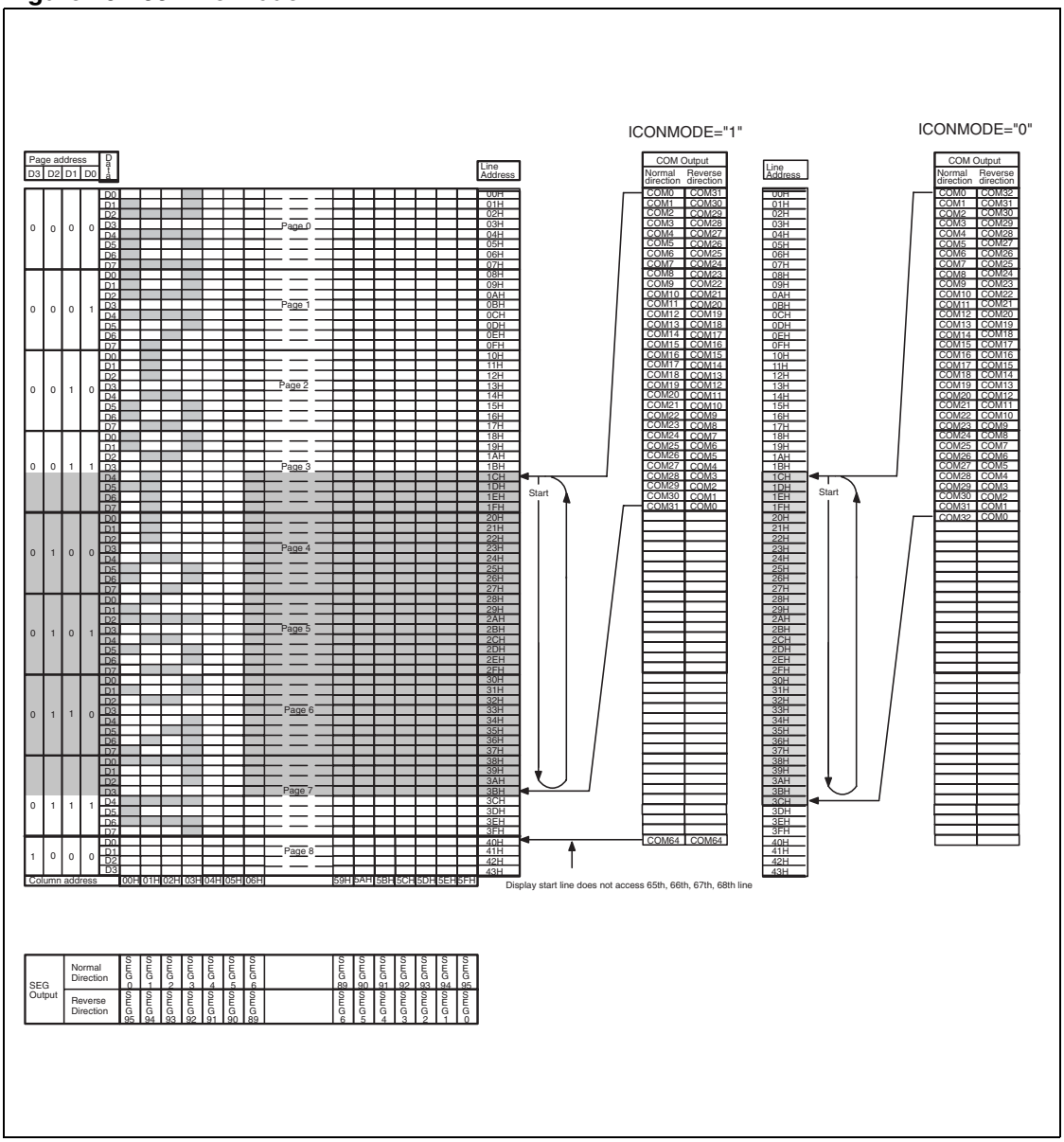


Figure 26. 33–line Mode



5.3 Partial Display

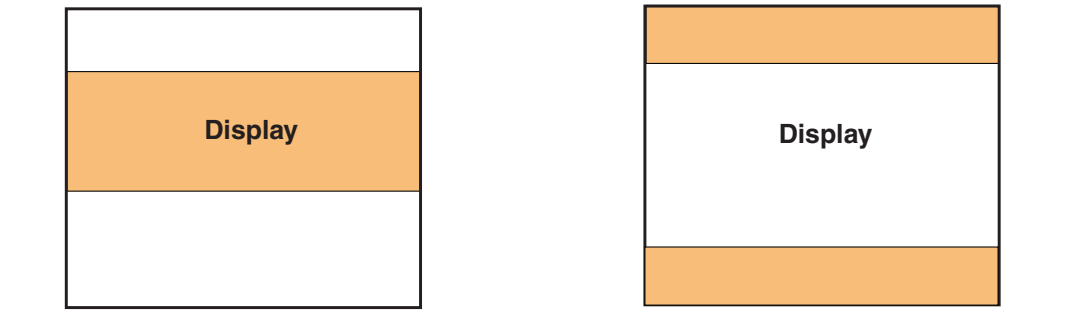
STE2007 feature four configuration for Partial Display function:

- 33 Line Partial Display
- 25 Line Partial display
- 16 Line Partial Display
- 9 Line Partial Display

Partial display Area location on the screen is defined by Image Location Parameter.

Image Location + Partial display area > Multiplexing rate.

Figure 27.



When Partial Display Mode is enabled the user has to Update the Operative Voltage, Bias Ratio and Charge Pump Setting to match the new working conditions.

5.3.1 33 Line Partial Display Mode

Partial Display Area is composed of 33 Lines. Memory vs. Row Drivers Mapping is defined according to the following parameters:

- Multiplexing Value
- IL[2:0]

Figure 28. Example: Partial Display 33 lines & MUX65

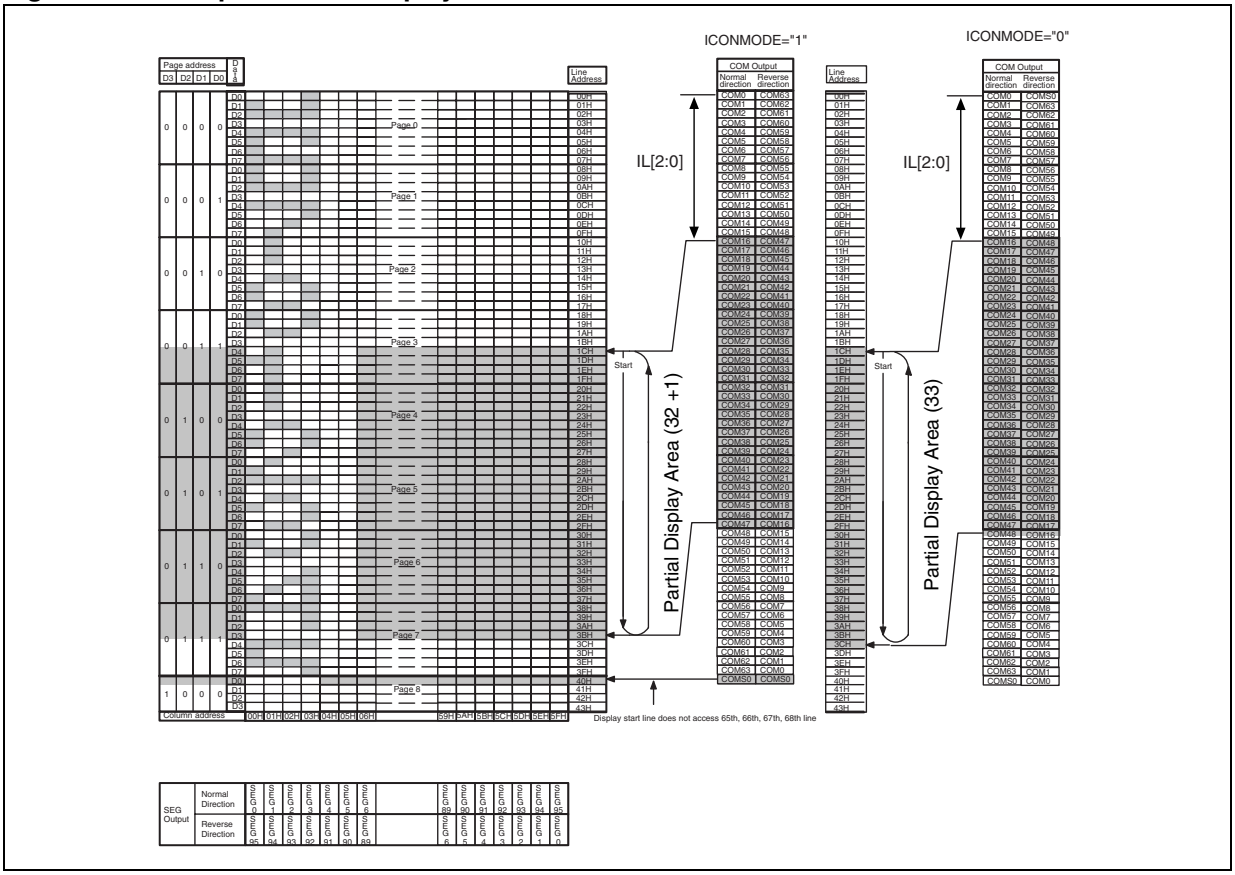
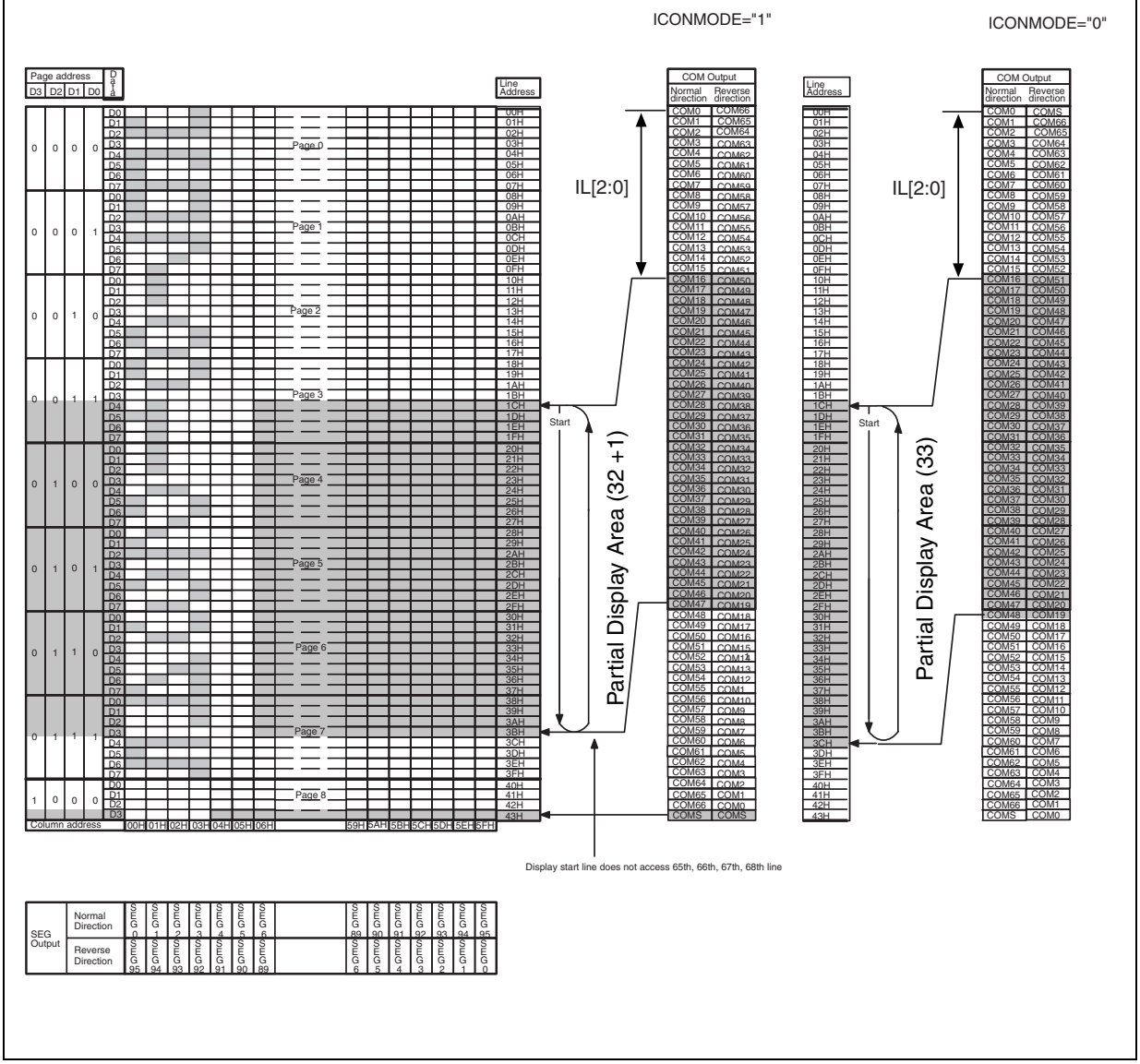


Figure 29. Example: Partial Display 33 lines & MUX68

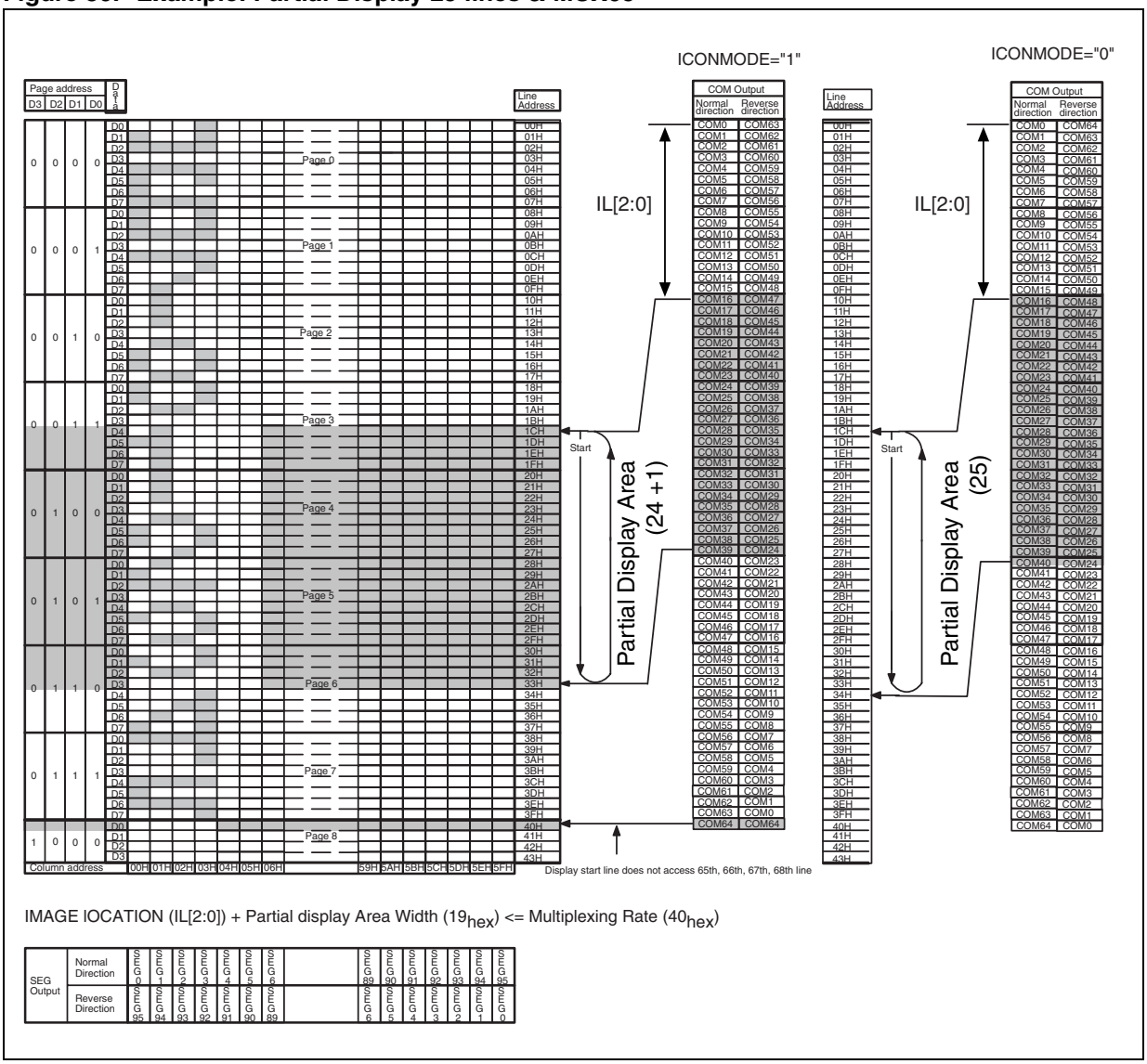


5.3.2 25 Line Partial Display Mode

Partial Display Area is composed of 25 Lines. Memory vs. Row Drivers Mapping is defined according to the following parameters:

- Multiplexing Value
- IL[2:0]

Figure 30. Example: Partial Display 25 lines & MUX65

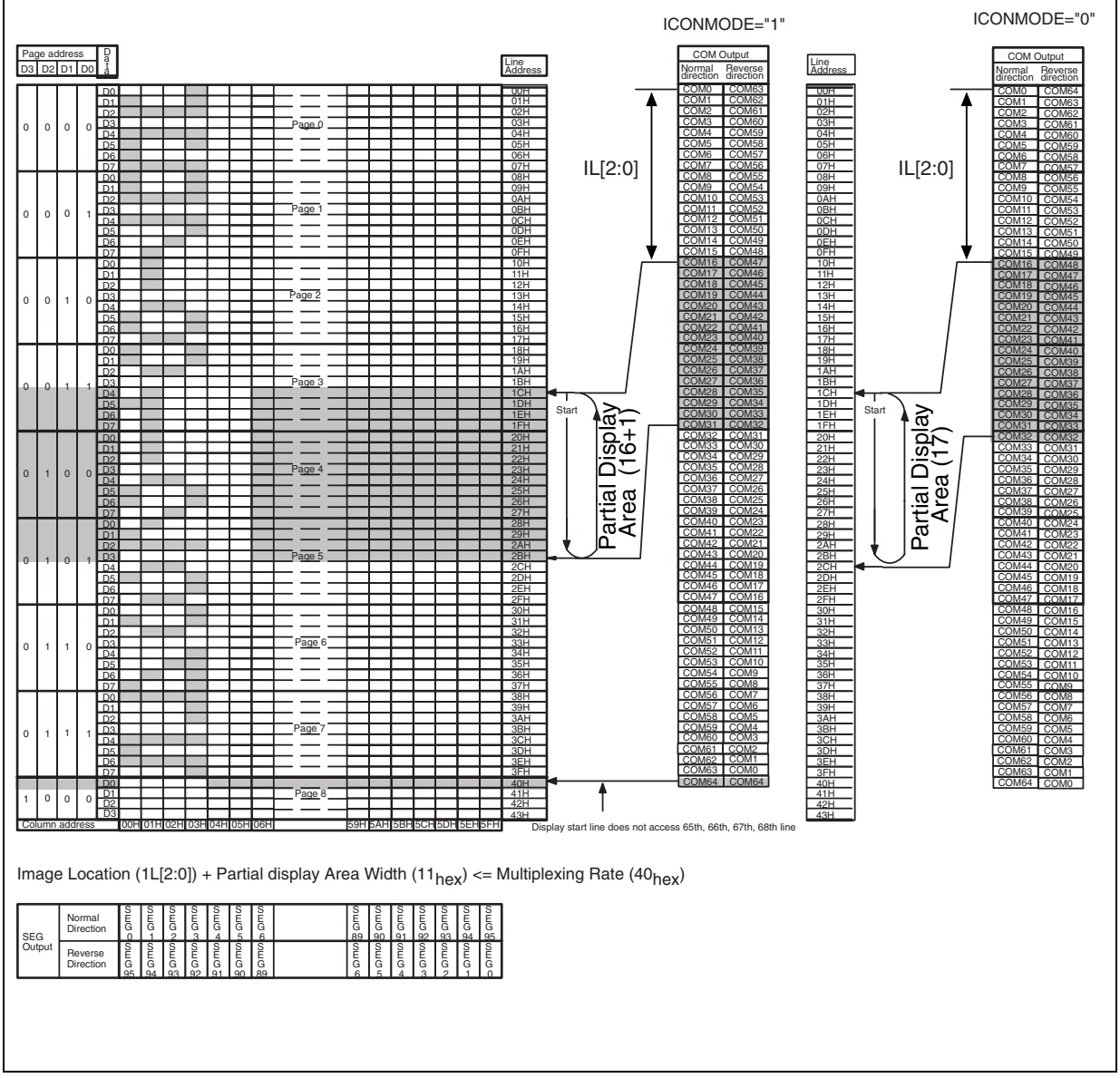


5.3.3 17 Line Partial Display Mode

Partial Display Area is composed of 17 Lines. Memory vs. Row Drivers Mapping is defined according to the following parameters:

- Multiplexing Value
- IL[2:0]

Figure 31. Partial Display 17 Lines

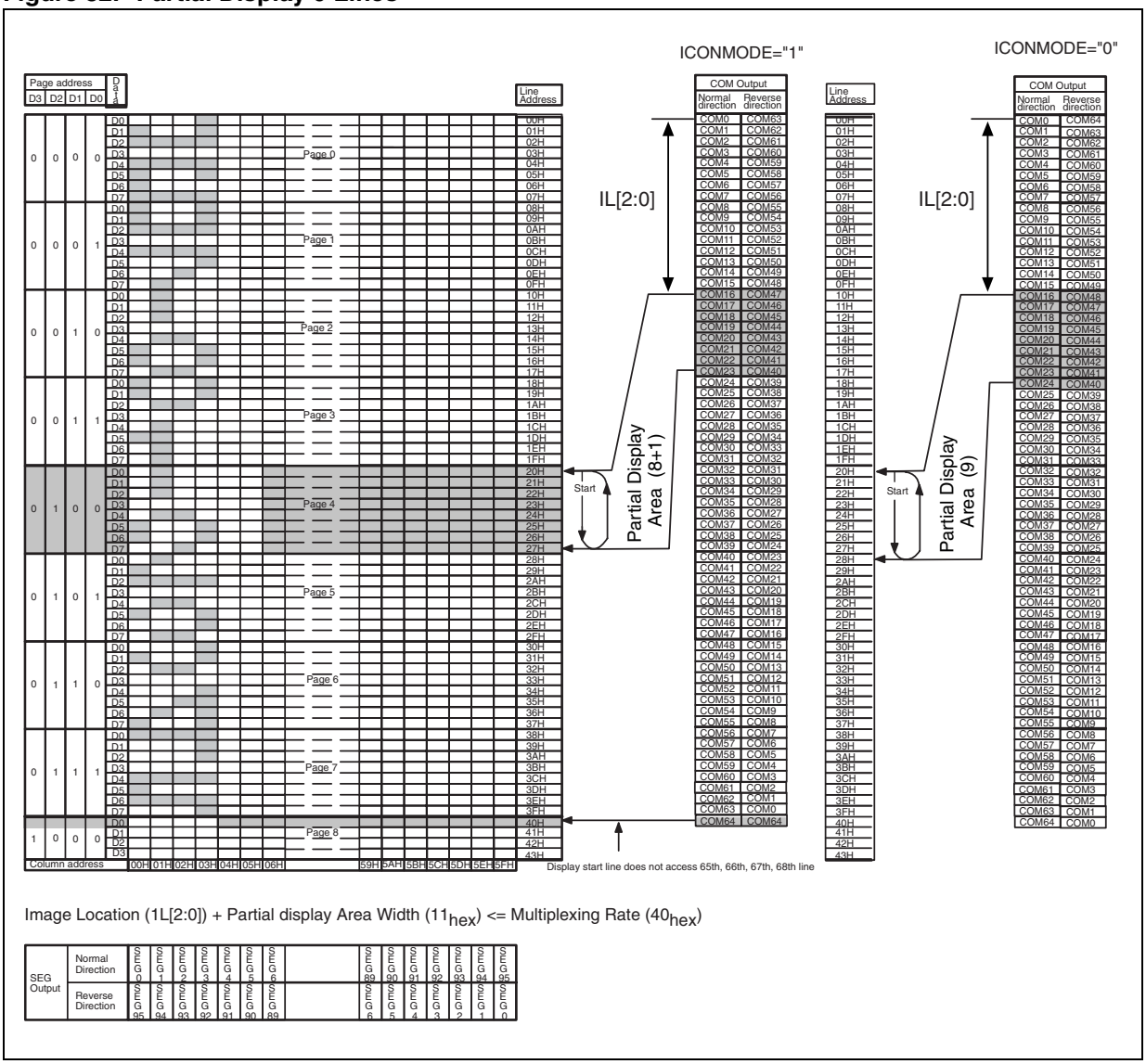


5.3.4 9 Line Partial Display Mode

Partial Display Area is composed of 9 Lines. Memory vs. Row Drivers Mapping is defined according to the following parameters:

- Multiplexing Value
- IL[2:0]

Figure 32. Partial Display 9 Lines



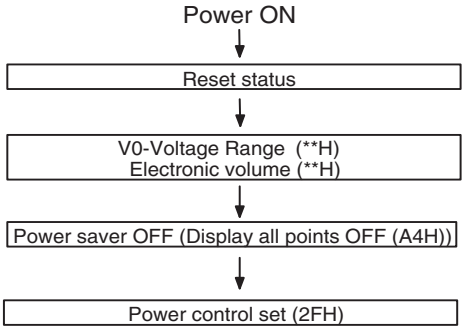
5.4 Command Parameters Default Configuration

Table 17.

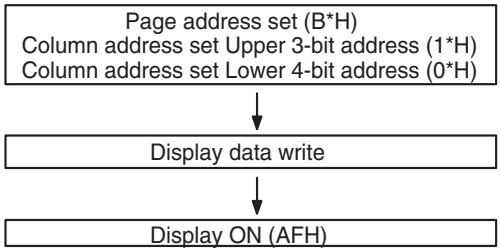
STATUS	After Power On	After HW Reset	After SW Reset	Description
Driver Status	MCU TxData–mode	MCU TxData–mode	MCU TxData–mode	
Power Saver Mode	Power Saver Mode	Power Saver Mode	Power Saver Mode	
DISPLAY MODE	All Pixel On	All Pixel On	All Pixel On	
INVERSION	OFF	OFF	OFF	
Display	OFF	OFF	OFF	
Frame Memory	Random	No Change	No Change	
Page Address	0hex	0hex	0hex	
Columns Address	0hex	0hex	0hex	
Display Start line	0hex	0hex	0hex	
Segment drivers Direction	Normal	Normal	Normal	
Common Drivers Direction	Normal	Normal	Normal	
VOR - Voltage Range	4hex	4hex	4hex	
Electronic Volume	90hex	90hex	90hex	
Power Control Register	Booster OFF	Booster OFF	Booster OFF	
ID byte	0hex	0hex	0hex	IDA/IDB Pads
Charge Pump	5x	5x	5x	
Bias Ratio	1/10	1/10	1/10	
VLCD Temeprature Comp.	0ppm	0ppm	0ppm	
N-Line Inversion	Frame Inv.	Frame Inv.	Frame Inv.	
Multiplexing Rate	1/68	1/68	1/68	
Refresh Rate	80Hz	80Hz	80Hz	
Image Location	0hex	0hex	0hex	
Icon Mode	Disabled	Disabled	Disabled	

6 Instruction Setups

6.1 Initialization (Power ON Sequence)

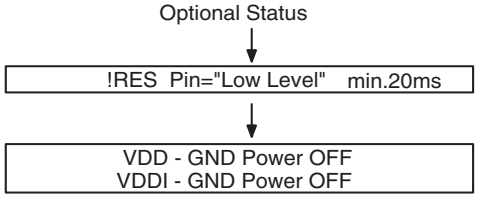


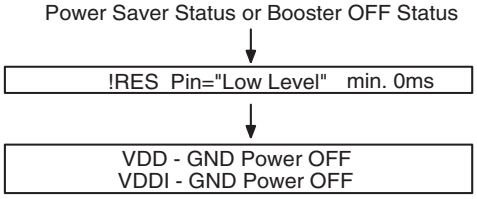
6.2 Display Data Writing Sequence


Page address set (B*H)
Column address set Upper 3-bit address (1*H)
Column address set Lower 4-bit address (0*H)
Display data write
Display ON (AFH)

This command is needed only at 1st time after initialization.

6.3 Power OFF

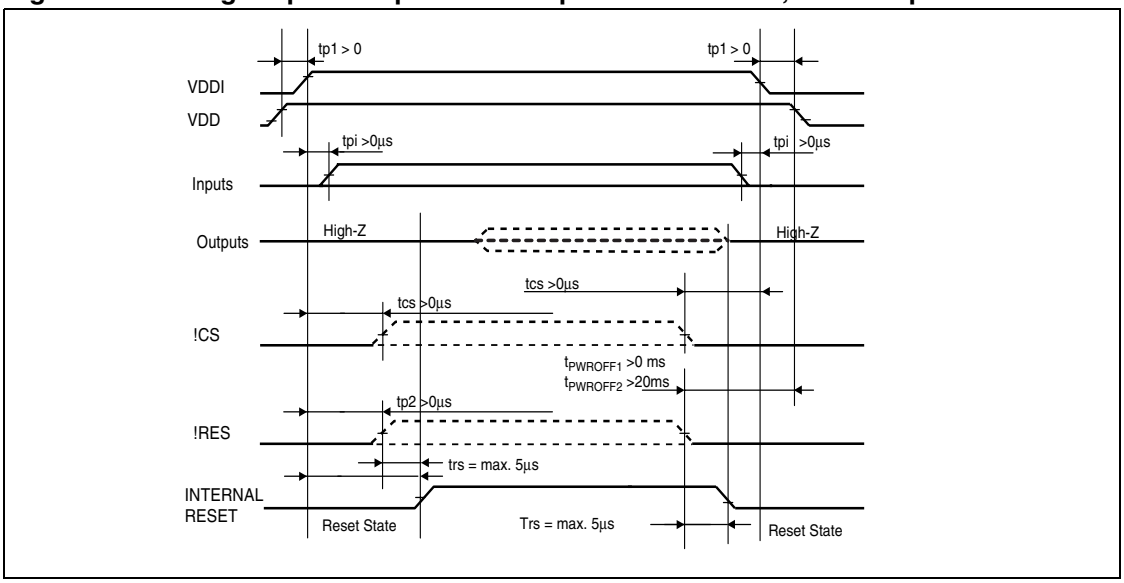




7 Power ON/Power OFF timing Sequence

In *Figure 33* is the timing diagram for power on/power down sequences.

Figure 33. Timing for phone's power on sequence when VDD,VDDCP Up before VDDI



XCS,SDAIN,XRES can become "High" simultaneously with VDDI (tcs>0,tpi>0;tp2>0).

trs= max 5000ns (Internal Reset Time- see AC Characteristics Paragraph)

$t_{PWROFF1}$>0ms must be considered when driver is in Power Saver or Booster OFF status

$t_{PWROFF2}$>20ms must be considered when driver is in Normal Working Condition

VDDI, VDD and VDD_CP can come up/go down in any sequence

VDDI can be Up with VDD, VDDCP down and viceversa. If only one supply rail is up, the driver is forced in reset state.

If VDD is high after VDDI all timing referred to VDDI must be referred to VDD (Fig. 24)

Figure 34. Timing for phone's power on sequence when VDDI Up before VDD

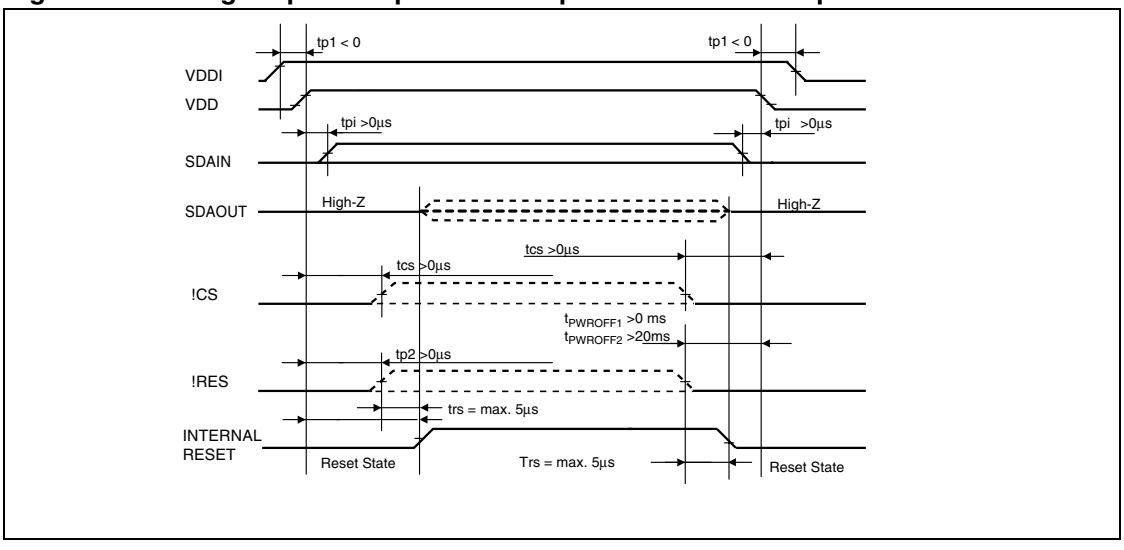


Table 18. Instruction Set

Command	Code										Function
	(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Display ON/OFF	0	1	0	1	0	1	1	1	0 1	AE AF	LCD display 0: OFF, 1: ON
Display normal/ reverse	0	1	0	1	0	0	1	1	0 1	A6 A7	LCD display 0: normal, 1: reverse
Display all points ON/ OFF	0	1	0	1	0	0	1	0	0 1	A4 A5	LCD display 0: normal display, 1: all points ON
Page address set	0	1	0	1	1	address					Sets the DDRAM page address
Column address set upper 3–bit address	0	0	0	0	1	*	address				Sets the DDRAM column address
Column address set lower 4–bit address	0	0	0	0	0	address					
Display start line address set	0	0	1	address							Sets the DDRAM display start line address
Segment driver direction	0	1	0	1	0	0	0	0	0 1	A0 A1	Sets the correspondence between the DDRAM column address and the SEG driver output. 0:Normal, 1: reverse
Common driver direction select	0	1	1	0	0	0 1	*	*	*		Sets the correspondence between the DDRAM line address and the COM driver output. 0: normal, 1: reverse
Display data write	1	Write data									Writes to the DDRAM
Self Test/Identification data reading	0	1	1	0	1	1	0	1	1	DB	Identification byte
Power control set	0	0	0	1	0	1	Operating mode				Sets the on–chip power supply circuit operating mode
VO-Range	0	0	0	1	0	0	VO-Range				Sets the electronic volume value
Electronic volume	0	1	0	0	Electronic volume value						Sets the electronic volume value
Power saver	–	–	–	–	–	–	–	–	–		Compound command of Display OFF and Display-all-points-ON
Reset	0	1	1	1	0	0	0	1	0	E2	Internal reset
NOP	0	1	1	1	0	0	0	1	1	E3	Non–operation
VOP	0	1	1	1	0	0	0	0	1	E1	Sets the VLCD
	0	VOP[7:0]									
Termal Compensation	0	0	0	1	1	1	0	0	0	38	SET VLCD Slope in temperature
	0	*	*	*	*	*	Thermal Comp				

Table 18. Instruction Set (continued)

Command	Code										Function
	(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Charge Pump	0	0	0	1	1	1	1	0	1	3D	Sets the Charge Pump Mux Factor
	0	*	*	*	*	*	*	Charge Pump			
Refresh Rate	0	1	1	1	0	1	1	1	1	EF	Sets the Display Refresh Frequency
	0	*	*	*	*	*	*	Refersh Rate			
Bias ratio	0	0	0	1	1	0	Bias Ratio				Sets the VLCD
N-line Inversion	0	1	0	1	0	1	1	0	1	AD	
	0	*	*	F1	N-Line Inversion						
Number of Lines	0	1	1	0	1	0	Mux Rate				
Image Location	0	1	0	1	0	1	1	0	0	AC	SET Initial Row on Display
	0	*	*	*	*	*	IL[2:0]				
Icon Mode	0	1	1	1	1	1	0	0	Icon		
STM TEST MODE1	0	1	0	1	0	1	0	0	1	A9	Reserved for STM (STM Test Mode)
	0	*	*	*	*	*	*	*	*		
STM TEST MODE2	0	1	0	1	0	1	0	1	0	AA	Reserved for STM (STM Test Mode)
STM TEST MODE3	0	1	0	1	0	1	0	1	1	AB	Reserved for STM (STM Test Mode)
STM TEST MODE4	0	1	0	1	0	1	0	0	0	A8	Reserved for STM (STM Test Mode)
STM TEST MODE5	0	1	1	1	1	1	1	1	1	FF	Reserved for STM (STM Test Mode)
STM TEST MODE6	0	1	1	1	1	1	1	0	0	FC	Reserved for STM (STM Test Mode)
STM TEST MODE7	0	1	1	1	1	1	1	1	0	FE	Reserved for STM (STM Test Mode)
STM TEST MODE8	0	1	1	1	1	1	1	0	1	FD	Reserved for STM (STM Test Mode)

* = Disabled bits.

8 Commands

8.1 Display ON/OFF

This command turns the display ON and OFF

Table 19. Display ON/OFF

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	1	0	1	0	1	1	1	0	AE	Display OFF
0								1	AF	Display ON

When the Display OFF command is executed in the Display all points ON mode, Power saver mode is entered. See the section on the Power saver for details.

8.2 Display normal/reverse

This command can reverse the lit and unlit without overwriting the contents of the DDRAM.

Table 20. Display normal/reverse

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	1	0	1	0	0	1	1	0	A6	Normal:DDRAM Data ”H”=LCD ON voltage
0								1	A7	Reverse:DDRAM Data ”L”=LCD ON voltage

8.3 Display all points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the DDRAM. Even when this is done, the DDRAM contents are maintained. This command takes priority over the Display normal/reverse command.

Table 21. Display all points ON/OFF

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	1	0	1	0	0	1	0	0	A4	Normal Display Mode
0								1	A5	Display All Points ON

When the Display all points ON command is executed when in the Display OFF mode, Power saver mode is entered. See the section on the Power Saver for details.

8.4 Page address set

This command specifies the page address of the DDRAM.

Specifying the page address and column address enables to access a desired bit of the DDRAM. After the last column address (5FH), page address is incremented by +1. After the very last address (column = 5FH, page = 8H), page address return to 0H.

Table 22. Page address set

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	1	0	1	1	0	0	0	0	B0	0H
0					0	0	0	1	B1	1H
0					0	0	1	0	B2	2H
0					:				:	:
0					1	0	0	0	B8	8H

8.5 Column address set

This command specifies the column address of the DDRAM. The column address is split into two sections (the upper 3–bits and lower 4–bits) when it is set.

Each time the DDRAM is accessed, the column address automatically increments by +1, imaging it possible for the MCU to continuously access to the display data. After the last column address (5FH), column address returns to 00H.

Table 23. Column address set

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	0	0	0	1	*	A6	A5	A4	Upper bit address
				0	A3	A2	A1	A0	Lower bit address

* Disabled bit

(D/C)	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
.				.				
.				.				
0	1	0	1	1	1	1	0	5EH
0	1	0	1	1	1	1	1	5FH

8.6 Display start line address set

This command is used to specify the display start line address of the DDRAM.

If the display start line address is changed dynamically using this command, then screen scrolling, page swapping can be performed.

Table 24. Display start line address set

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	0	1	0	0	0	0	0	0	40	0H
0	0	1	0	0	0	0	0	1	41	1H
0	0	1	0	0	0	0	1	0	42	2H
:					:					:
0	0	1	1	1	1	1	1	0	7E	3EH
0	0	1	1	1	1	1	1	1	7F	3FH

Display start line assress con be used in partial dispaly mode to relocate the partial display window on the screen.

Display start line + Partial Display area with must be smaller or equal to the number of line selected.

8.7 Segment driver direction select

This command can reverse the correspondence between the DDRAM column address and the segment driver output.

Table 25. Segment driver direction select

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	1	0	1	0	0	0	0	0	A0	Normal
0								1	A1	Reverse

8.8 Common driver direction select

This command can reverse the correspondence between the DDRAM line address and the common driver output.

Table 26. Common driver direction select

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	1	0	0	0	*	*	*	Normal
					1	*	*	*	Reverse

* Disabled bit

8.9 Display data write

This command writes 8–bit data to the specified DDRAM address. Since the column address is automatically incremented by +1 after each write, the MCU can continuously write multiple–word data.

Table 27. Display data write

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0
1	Write Data							

8.10 Data reading from driver (Driver TxData–mode)

These commands set SDAOUT to Driver TxData–mode and enable to read the identification byte.

Table 28. ID Byte

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	1	1	0	1	1	0	1	1	DB	Reads ID byte
0	0	0	IDB	IDA	0	0	0	0		Pad Default

8.11 Power Control Set

This command sets the on–chip power supply function ON/OFF.

Table 29. Power Control Set

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Setting
0	0	0	1	0	1	0	0	0	28	Booster : OFF Voltage Regulator:OFF Voltage Follower : OFF
0						0	0	1	29	
0						0	1	0	2A	
0						0	1	1	2B	
0						1	0	0	2C	
0						1	0	1	2D	
0						1	1	0	2E	
0						1	1	1	2F	Booster : ON Voltage regulator : ON Voltage follower : ON

8.12 VLCD set

The LCD Voltage VLCD at reference temperature (T_A = 25°C) can be set using the Voltage Range V0R, Electronic Volume EV and VOP registers content according to the following formula:

$$VLCD\ (T=T_A) = (\ V0P[7:0] + EV[4:0] - 16 + 32 \cdot V0R[2:0]) \cdot B + VLCD_{MIN}$$

with the following values:

Symbol	Value	Unit	Note
B	0.04	V	Single Voltage Step
$VLCD_{MIN}$	3	V	
T_A	25	°C	Room Temperature

For information on VLCD thermal compensation see PAR. 8.18 .

Figure 35.

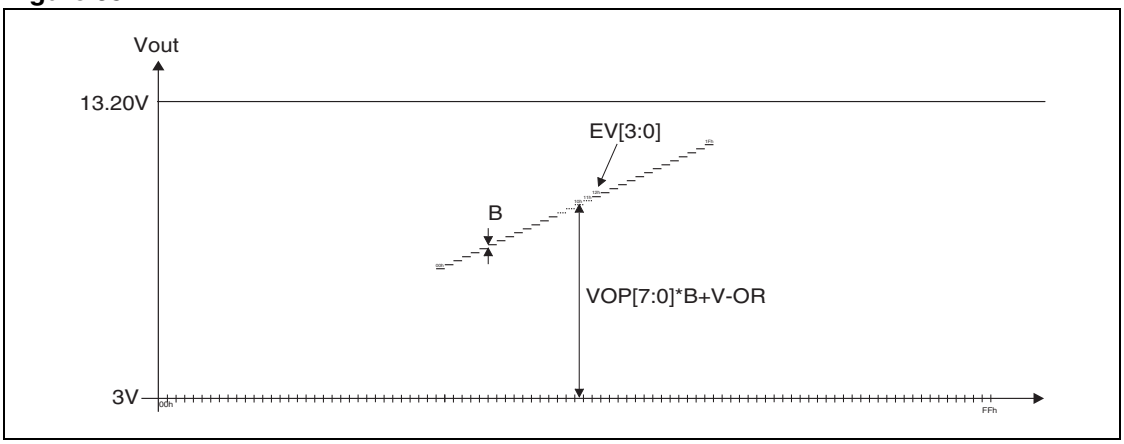
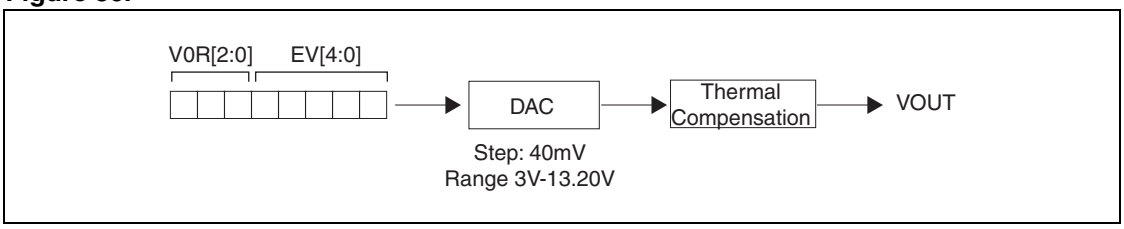


Figure 36.



8.12.1 V0R - Voltage Range Set

This command sets a value of the Voltage Range.

Table 30. V0R – Voltage Range

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	0	0	1	0	0	V0R - Voltage Range			Command Identifier + Data Field

Table 31. V0R

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	V0R Value	$32 \cdot V0R \cdot B + VLCD_{MIN}$
0	0	0	1	0	0	0	0	0	20	0	3.00 V
0						0	0	1	21	1	4.28 V
0						0	1	0	22	2	5.56 V
0						0	1	1	23	3	6.84 V
0						1	0	0	24	4	8.12 V (Default)
0						1	0	1	25	5	9.40 V
0						1	1	0	26	6	10.68 V
0						1	1	1	27	7	11.96 V

8.12.2 VOP Set

Contrast Setting Adjustment .

Table 32. VOP Set

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	1	1	1	0	0	0	0	1	E1	Command Identifier
0	VOP7	VOP6	VOP5	VOP4	VOP3	VOP2	VOP1	VOP0		Data Field

Table 33. VOP

VOP7	VOP6	VOP5	VOP4	VOP3	VOP2	VOP1	VOP0	HEX	VOP Adjustment
0	0	0	0	0	0	0	0	00	0 Step (Default)
0	0	0	0	0	0	0	1	01	+1 Step
0	0	0	0	0	0	1	0	02	+2 Step
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	7F	+127 Step
1	0	0	0	0	0	0	0	80	0 Step
1	0	0	0	0	0	0	1	81	-1 Step
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	FD	-125 Step
1	1	1	1	1	1	1	0	FE	-126 Step
1	1	1	1	1	1	1	1	FF	-127 Step

8.12.3 Electronic volume

This command sets a value of electronic volume EV for the VLCD voltage regulator, to adjust the contrast of LCD panel display (End User).

Table 34. Electronic volume

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	Electronic Volume Value					Command Identifier + Data Field

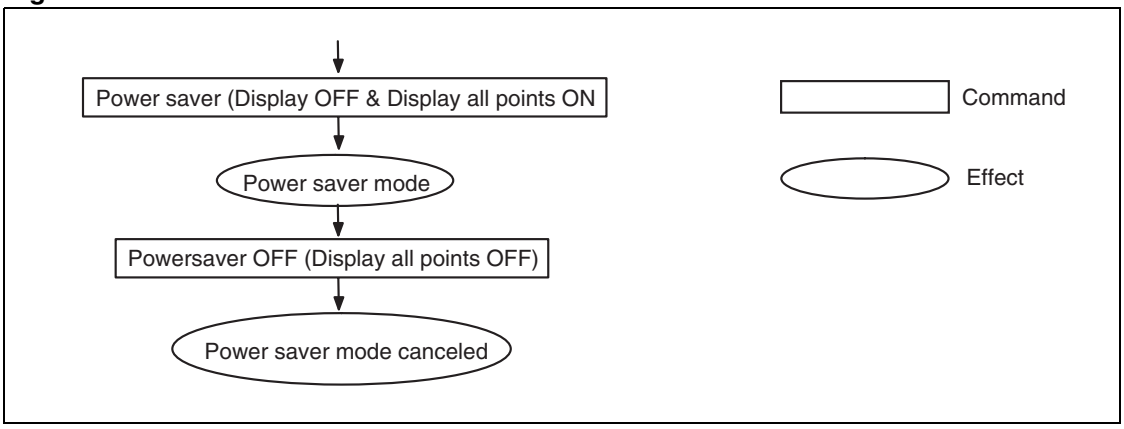
Table 35. EV

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Hex	EV Value	VLCD voltage
0	1	0	0	0	0	0	0	0	80	0 Step	low
0				0	0	0	0	1	81	1 Step	
0				0	0	0	1	0	82	2 Step	
:						:			:	:	:
0				1	0	0	0	0	90	16 Step (Default)	
:						:			:	:	:
0				1	1	1	1	0	9E	30 Step	
0				1	1	1	1	1	9F	31 Step	high

8.13 Power saver mode

If the display all points ON command is executed when the display is in display OFF mode, power saver mode is entered. This mode stops every operation of the LCD display system.

Figure 37. Power saver mode


Power saver (Display OFF & Display all points ON
Power saver mode
Powersaver OFF (Display all points OFF)
Power saver mode canceled
Command
Effect

The internal states in power saver mode are as follows:

- The oscillation circuit is stopped
- The LCD power supply circuit is stopped
- The LCD driver circuit is stopped and segment/common driver outputs to the Vss level

– The display data and operation mode before execution of the Power saver are held, and the MCU can access to the DDRAM and internal registers.

8.14 Reset

When this command is issued, the driver is initialized.This command doesn't change DDRAM content.

Table 36. Reset

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	1	1	1	0	0	0	1	0	E2	Command Identifier

8.15 NOP

Non–operation command.

Table 37. NOP

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	1	1	1	0	0	0	1	1	E3	Command Identifier

8.16 Image Location

Image Location Command

Table 38. Image Location

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	1	0	1	0	1	1	0	0	AC	Command Identifier
0	*	*	*	*	*	IL2	IL1	IL0		Data Field

Table 39. Image Location

IL2	IL1	IL0	Function
0	0	0	0 Lines
0	0	1	8 Lines
0	1	0	16 Lines
0	1	1	24 Lines
1	0	0	32 Lines
1	0	1	48 Lines
1	1	0	56 Lines
1	1	1	64 Lines

8.17 Bias Ratio

It is possible to select different Bias Ratio.

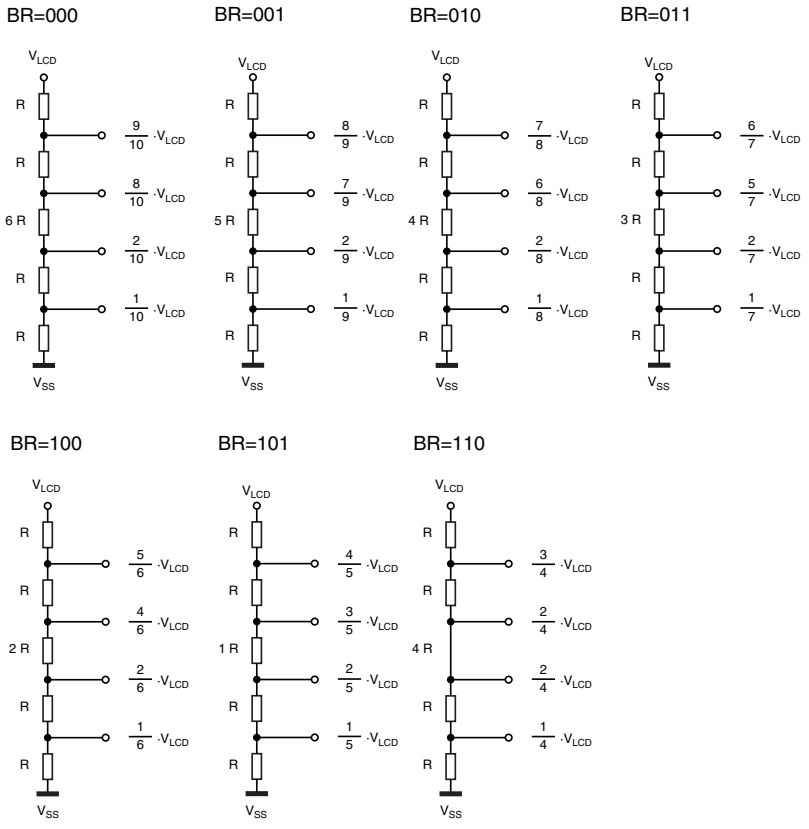
Table 40. Bias Ratio

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	1	1	0	BR2	BR1	BR0	Command Identifier + Data Field

Table 41. BIAS Ratio

BR2	BR1	BR0	Function
0	0	0	Bias Ratio =1/10 - 81 Lines
0	0	1	Bias Ratio = 1/9 - 65 Lines
0	1	0	Bias Ratio =1/8 - 49 Lines
0	1	1	Bias Ratio = 1/7 - 33 Lines
1	0	0	Bias Ratio =1/6 - 25 Lines
1	0	1	Bias Ratio = 1/5 - 17 Lines
1	1	0	Bias Ratio =1/4 - 9 Lines
1	1	1	Not Used

Table 42. Bias levels Generator



8.18 Temperature Compensation

Its is possible to select different VLCD temperature compensation Coefficients.

Table 43. VLCD Temperature Compensation

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	0	0	1	1	1	0	0	0	38	Command Identifier
0	*	*	*	*	*	Thermal Compensation TC				Data Field

Temperature Compensation Formula:

$$VLCD(T) = VLCD(T_A) \cdot [1 + (T(°C) - T_A) \cdot TC]$$

TC = Temperature Compensation Coefficients

T(°C) = Temperature

$VLCD(T_A)$ = LCD Voltage at T_A Temperature (Room Temperature)

Table 44. TC

TC2	TC1	TC0	TC Value
0	0	0	TC= 0 PPM
0	0	1	TC= -300 PPM
0	1	0	TC= -600 PPM
0	1	1	TC= -900 PPM
1	0	0	TC= -1070 PPM
1	0	1	TC= -1200 PPM
1	1	0	TC= -1500 PPM
1	1	1	TC= -1800 PPM

8.19 Charge Pump Multiplication Factor

It is possible to select different Charge Pump Multiplication Factors.

Table 45. Charge Pump Setting

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	0	0	1	1	1	1	0	1	3D	Command Identifier
0	*	*	*	*	*	*	CP1	CP0		Data Field

Table 46. Charge Pump Multiplication Factor

CP1	CP0	Function
0	0	5 x
0	1	4 x
1	0	3 x
1	1	Not Used

8.20 Refresh Rate

It is possible to select different Refresh Rate.

Table 47. Refresh Rate

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	1	1	1	0	1	1	1	1	EF	Command Identifier
0	*	*	*	*	*	*	RR1	RR0		Data Field

Table 48. Refresh Rate

RR1	RR0	Function
0	0	80 Hz
0	1	75 Hz
1	0	70 Hz
1	1	65 hz

8.21 Icon Mode

Icon Mode

- 0: Icon Mode Disabled
- 1: Icon Mode Enabled

Table 49. Icon Mode

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Function
0	1	1	1	1	1	0	0	ICON	Command Identifier

8.22 N- Line Inversion

N-line Inversion Function.

Table 50. N-Line Inversion

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Function
0	1	0	1	0	1	1	0	1	AD	Command Identifier
0	*	*	F1	NL4	NL3	NL2	NL1	NL0		Data Field

Table 51. N-Line

F1	NL4	NL3	NL2	NL1	NL0	Function	N row
*	0	0	0	0	0	N-line inversion disabled (default)	
0	*	*	*	*	*	XOR function disabled	
1	*	*	*	*	*	XOR function enabled	
*	0	0	0	0	1	N-line inversion enabled	2
*	0	0	0	1	0	N-line inversion enabled	3
:	:	:	:	:	:	:	:
*	1	1	1	1	1	N-line inversion enabled	32

The XOR function defines the polarity as the result of the logical XOR between the N-Line and the frame polarity.

8.23 Number of Lines

Multiplexing Rate setting command.

Table 52. Number of Lines

(D/C)	D7	D6	D5	D4	D3	D2	D1	D0	Function
0	1	1	0	1	0	M2	M1	M0	Command Identifier + Data Field

Table 53. Multiplexing Rate

M2	M1	M0	Function
0	0	0	68 Lines (Default)
0	0	1	65 Lines
0	1	0	49 Lines
0	1	1	33 Lines
1	0	0	33 Lines Partial Display
1	0	1	25 Lines Partial Display
1	1	0	17 Lines Partial Display
1	1	1	9 Lines Partial Display

9 Chip Mechanical Drawing

Table 54. Mechanical Dimensions

Parameter	Dimensions
Wafer Thickness	500µm
Die Size (X x Y)	5.92 mm x 1.29 mm
Bumps Size on Columns and Segments Side	28µm X 89 µm X 15
Pad Size on Columns and Segments Side	35µm X 96µm
Bumps Pitch on Columns and Segments Side	45µm
Bumps Size on Interfaces Side	55µm X 73µm X 15
Pad Size on Interfaces Side	64 µm X 82 µm
Bumps Pitch on Interfaces Side	72µm
Spacing between Bumps	17µm

Table 55. Pad Coordinates

NAME	PAD	X (µm)	Y(µm)
R16	1	-2632.5	-514.35
R14	2	-2587.5	-514.35
R12	3	-2542.5	-514.35
R10	4	-2497.5	-514.35
R8	5	-2452.5	-514.35
R6	6	-2407.5	-514.35
R4	7	-2362.5	-514.35
R2	8	-2317.5	-514.35
R0	9	-2272.5	-514.35
C0	10	-2227.5	-514.35
C1	11	-2182.5	-514.35
C2	12	-2137.5	-514.35
C3	13	-2092.5	-514.35
C4	14	-2047.5	-514.35
C5	15	-2002.5	-514.35
C6	16	-1957.5	-514.35
C7	17	-1912.5	-514.35
C8	18	-1867.5	-514.35
C9	19	-1822.5	-514.35
C10	20	-1777.5	-514.35
C11	21	-1732.5	-514.35
C12	22	-1687.5	-514.35
C13	23	-1642.5	-514.35
C14	24	-1597.5	-514.35
C15	25	-1552.5	-514.35
C16	26	-1507.5	-514.35
C17	27	-1462.5	-514.35
C18	28	-1417.5	-514.35

Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
C19	29	-1372.5	-514.35
C20	30	-1327.5	-514.35
C21	31	-1282.5	-514.35
C22	32	-1237.5	-514.35
C23	33	-1192.5	-514.35
C24	34	-1147.5	-514.35
C25	35	-1102.5	-514.35
C26	36	-1057.5	-514.35
C27	37	-1012.5	-514.35
C28	38	-967.5	-514.35
C29	39	-922.5	-514.35
C30	40	-877.5	-514.35
C31	41	-832.5	-514.35
C32	42	-787.5	-514.35
C33	43	-742.5	-514.35
C34	44	-697.5	-514.35
C35	45	-652.5	-514.35
C36	46	-607.5	-514.35
C37	47	-562.5	-514.35
C38	48	-517.5	-514.35
C39	49	-472.5	-514.35
C40	50	-427.5	-514.35
C41	51	-382.5	-514.35
C42	52	-337.5	-514.35
C43	53	-292.5	-514.35
C44	54	-247.5	-514.35
C45	55	-202.5	-514.35
C46	56	-157.5	-514.35

Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
C47	57	-112.5	-514.35
C48	58	112.5	-514.35
C49	59	157.5	-514.35
C50	60	202.5	-514.35
C51	61	247.5	-514.35
C52	62	292.5	-514.35
C53	63	337.5	-514.35
C54	64	382.5	-514.35
C55	65	427.5	-514.35
C56	66	472.5	-514.35
C57	67	517.5	-514.35
C58	68	562.5	-514.35
C59	69	607.5	-514.35
C60	70	652.5	-514.35
C61	71	697.5	-514.35
C62	72	742.5	-514.35
C63	73	787.5	-514.35
C64	74	832.5	-514.35
C65	75	877.5	-514.35
C66	76	922.5	-514.35
C67	77	967.5	-514.35
C68	78	1012.5	-514.35
C69	79	1057.5	-514.35
C70	80	1102.5	-514.35
C71	81	1147.5	-514.35
C72	82	1192.5	-514.35
C73	83	1237.5	-514.35
C74	84	1282.5	-514.35

Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
C75	85	1327.5	-514.35
C76	86	1372.5	-514.35
C77	87	1417.5	-514.35
C78	88	1462.5	-514.35
C79	89	1507.5	-514.35
C80	90	1552.5	-514.35
C81	91	1597.5	-514.35
C82	92	1642.5	-514.35
C83	93	1687.5	-514.35
C84	94	1732.5	-514.35
C85	95	1777.5	-514.35
C86	96	1822.5	-514.35
C87	97	1867.5	-514.35
C88	98	1912.5	-514.35
C89	99	1957.5	-514.35
C90	100	2002.5	-514.35
C91	101	2047.5	-514.35
C92	102	2092.5	-514.35
C93	103	2137.5	-514.35
C94	104	2182.5	-514.35
C95	105	2227.5	-514.35
R1	106	2272.5	-514.35
R3	107	2317.5	-514.35
R5	108	2362.5	-514.35
R7	109	2407.5	-514.35
R9	110	2452.4	-514.35
R11	111	2497.5	-514.35
R13	112	2542.5	-514.35

Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
R15	113	2587.5	-514.35
R17	114	2632.5	-514.35
R19	115	2831.85	-450.0
R21	116	2831.85	-405.0
R23	117	2831.85	-360.0
R25	118	2831.85	-315.0
R27	119	2831.85	-270.0
R29	120	2831.85	-225.0
R31	121	2831.85	-180.0
R33	122	2831.85	-135.0
R35	123	2831.85	-90.0
R37	124	2831.85	-45.0
R39	125	2831.85	0.0
R41	126	2831.85	45.0
R43	127	2831.85	90.0
R45	128	2831.85	135.0
R47	129	2831.85	180.0
R49	130	2831.85	225.0
R51	131	2831.85	270.0
R53	132	2831.85	315.0
R55	133	2831.85	360.0
R57	134	2831.85	405.0
R59	135	2831.85	450.0
R61	136	2632.5	514.35
R63	137	2587.5	514.35
R65	138	2542.0	514.35
R67	139	2497.5	514.35
TEST3	140	2376.0	517.5

Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
TEST4	141	2304.0	517.5
VSS_AUX	142	1944.0	517.5
VSS_AUX	143	1872.0	517.5
VSS_AUX	144	1800.0	517.5
VSS_AUX	145	1728.0	517.5
N_RES	146	1584.0	517.5
N_CS	147	1512.0	517.5
T2	148	1368.0	517.5
T1	149	1296.0	517.5
T0	150	1224.0	517.5
VSS	151	1152.0	517.5
VSS	152	1080.0	517.5
VSS	153	1008.0	517.5
VSS_LCD	154	936.0	517.5
VSS_LCD	155	864.0	517.5
VSS_LCD	156	792.0	517.5
VSS_CP	157	720.0	517.5
VSS_CP	158	648.0	517.5
VSS_CP	159	576.0	517.5
DC	160	432.0	517.5
SDAOUT	161	360.0	517.5
SDIN	162	288.0	517.5
SDOUT	163	216.0	517.5
SCLK	164	144.0	517.5
VREF_BUFF	165	72.0	517.5
VSS_AUX	166	-72.0	517.5
SEL1	167	-144.0	517.5
SEL0	168	-216.0	517.5

Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
SA1	169	-288.0	517.5
SA0	170	-360.0	517.5
IDB	171	-432.0	517.5
IDA	172	-504.0	517.5
OSC_IN	173	-576.0	517.5
VDDI	174	-720.0	517.5
VDDI	175	-792.0	517.5
VDDI	176	-864.0	517.5
VDDI	177	-936.0	517.5
VDDI	178	-1008.0	517.5
VDDI	179	-1080.0	517.5
VDD	180	-1224.0	517.5
VDD	181	-1296.0	517.5
VDD	182	-1368.0	517.5
VDD	183	-1440.0	517.5
VDD	184	-1512.0	517.5
VDD	185	-1584.0	517.5
VDD_CP	186	-1656.0	517.5
VDD_CP	187	-1728.0	517.5
VLCD_SNS	188	-1872.0	517.5
VLCD	189	-1944.0	517.5
VLCD	190	-2016.0	517.5
VLCD	191	-2088.0	517.5
VLCD	192	-2160.0	517.5
TEST4	193	-2304.0	517.5
TEST5	194	-2376.0	517.5
R66	195	-2497.5	514.35
R64	196	-2542.5	514.35

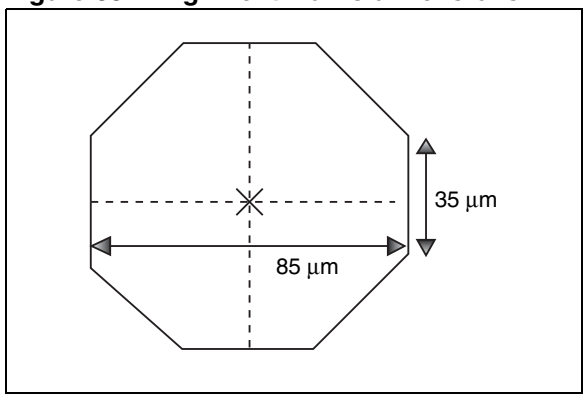
Table 55. Pad Coordinates (continued)

NAME	PAD	X(µm)	Y(µm)
R62	197	-2587.5	514.35
R60	198	-2632.5	514.35
R58	199	-2831.85	450.0
R56	200	-2831.85	405.0
R54	201	-2831.85	360.0
R52	202	-2831.85	315.0
R50	203	-2831.85	270.0
R48	204	-2831.85	225.0
R46	205	-2831.85	180.0
R44	206	-2831.85	135.0
R42	207	-2831.85	90.0
R40	208	-2831.85	45.0
R38	209	-2831.85	0.0
R36	210	-2831.85	-45.0
R34	211	-2831.85	-90.0
R32	212	-2831.85	-135.0
R30	213	-2831.85	-180.0
R28	214	-2831.85	-225.0
R26	215	-2831.85	-270.0
R24	216	-2831.85	-315.0
R22	217	-2831.85	-360.0
R20	218	-2831.85	-405.0
R18	219	-2831.85	-450.0

Table 56. Alignment marks coordinates

MARKS	X	Y
Mark1	-2834.55	517.05
Mark2	2834.55	517.05
Mark3	-2834.55	-517.05
Mark4	2834.55	-517.05
Mark5	2205.0	517.05

Figure 38. Alignment marks dimensions



10 Revision history

Date	Revision	Changes
9-Nov-2005	1	Initial release.

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